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VARIAN ASSOCIATES PALO ALTO CALIF CENTRAL RESEARCH LAB  
INDIUM PHOSPHIDE GUNN DEVICES (26-60 GHZ). (U)  
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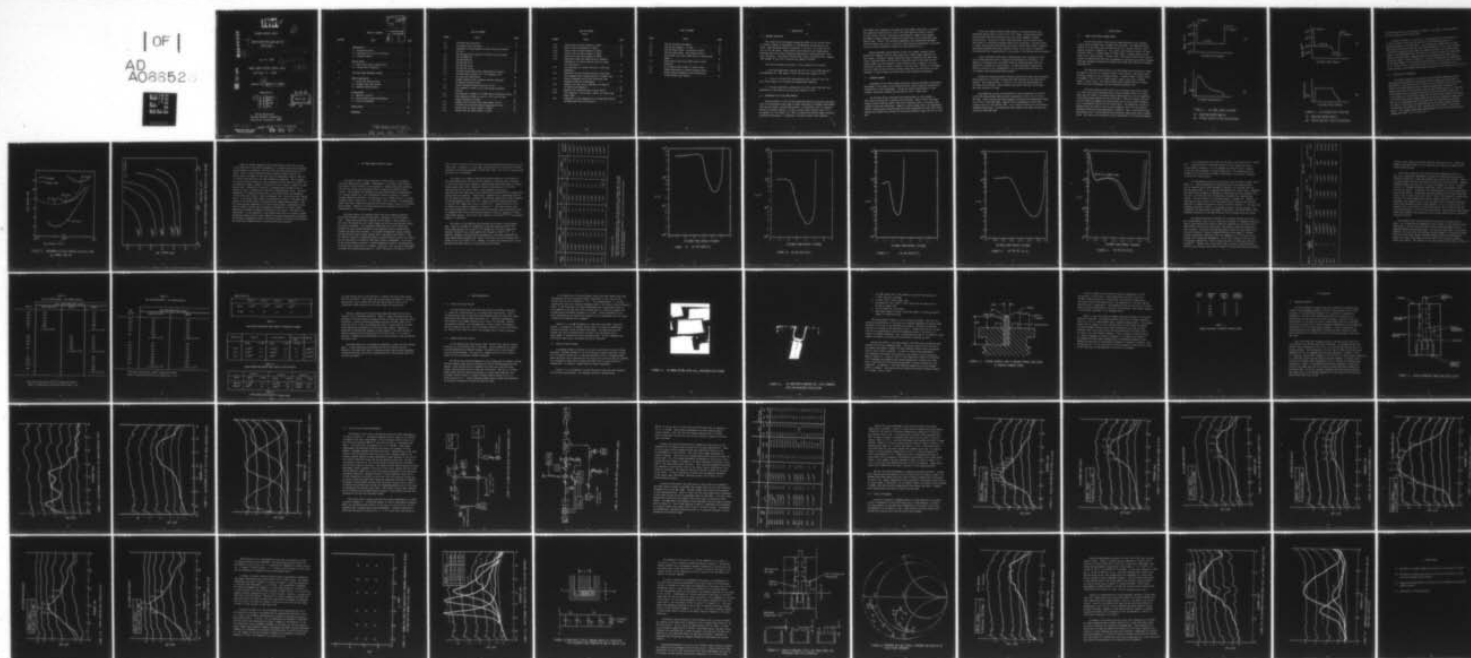
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SECOND INTERIM REPORT

*1st N/R*

INDIUM PHOSPHIDE GUNN DEVICES  
(25-60 GHz)

Interim rept. no. 2, 1 Jan-30 Jun 78,

JULY 27, 1978

11 27 Jul 78

NAVAL OCEAN SYSTEMS CENTER (NOSC)

SAN DIEGO, CA 92152

12 69p.

CONTRACT No. N00123-77-C-0459

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## 1. INTRODUCTION

### 1.1 PROGRAM OBJECTIVES

The research and development program described in this interim report is directed towards the development of InP materials and devices for low noise, broad bandwidth amplifier operation in the 26.5 to 40.0 GHz and the 40.0 to 60.0 GHz bands. These efforts were initiated by the Semiconductor Microwave R&D Group, Central Research Laboratories, Varian Associates, Palo Alto, California. This second interim report covers the period from 1 January 1978 through 30 June 1978 on Contract No. N00123-77-C-0459.

The final performance objectives of this program are as follows:

1. Low noise amplifiers covering the full 26.5 to 40.0 GHz band with the bandwidths of 7 GHz, gains of  $20 \pm 2$  dB and noise figures of 8 dB.
2. A 26.5 to 40.0 GHz full band amplifier with a gain of  $20 \pm 2$  dB and a noise figure of 8 dB using the staggered gain approach.
3. Low noise amplifiers covering the full 40.0 to 60.0 GHz band with bandwidths of 10%, gains of 6 dB and noise figures of 9 dB.

### 1.2 ADVANTAGES OF InP FOR GUNN DEVICES

The application of InP for CW transferred electron oscillators and amplifiers in the millimeter wave range provides significant performance improvements over the more widely utilized GaAs devices. In particular, InP is a superior material in several respects. It has a current peak-to-valley ratio of 3.5 as opposed to 2.5 for GaAs [1]. This, in theory will provide higher oscillator conversion efficiencies. In addition, the peak-to-valley ratio degrades

less rapidly with temperature than GaAs and the thermal conductivity is greater, thus favoring CW operation [2]. Due to the high effective transit velocity ( $1.3 \times 10^7$  cm/sec) and fast intervalley scattering [3], longer active regions and higher ultimate frequency limitations should favor InP for millimeter wave applications. Finally, InP reflection amplifiers have demonstrated extremely low noise figures (as low as 7.5 dB) [4], which have been attributed to the lower ratio of electron diffusion to mobility in this material [5].

Another important characteristic of InP is its higher threshold field. Because the threshold field is three times that of GaAs, power densities are much higher. Therefore, thermal limitations under CW operation are more significant, limiting practical CW devices to operation above 18 GHz (where active region lengths are short enough to permit effective heat transfer) or to bias polarities in which the anode is located at the heat sink. Because of the higher electric fields and more critical thermal interactions, CW InP devices are more dependent on bias voltage and current levels than equivalent GaAs devices.

### 1.3 PROGRESS SUMMARY

Achievement of the above program objectives requires extensive technological advancement in the areas of InP epitaxial growth, device design and fabrication, and amplifier circuit development. During the second interim period of this program, significant progress has been made in each of these areas.

Two InP Gunn device structures are being employed in this program, a three layer structure and a cathode notch structure. Both of these structures require several uniformly doped, high purity epitaxial layers to be grown under carefully controlled conditions. Based on a device design effort and experimental results, doping profile specifications have been established for both triple layer devices and cathode notch devices for the entire frequency range from 26.5 to 60.0 GHz.

An InP vapor phase epitaxial (VPE) reactor is operational which has background doping levels in the low  $10^{13} \text{ cm}^{-3}$  range. An  $\text{H}_2\text{S}$  doping system and procedures have been developed which allow rapid changes in doping concentrations. During this second reporting period, this VPE reactor has been devoted to exclusively growing cathode notch structures. Thirteen wafers of device quality were grown during this period. Several VPE process techniques and growth parameters have been studied in detail in an effort to establish controllability and reproducibility in the growth of InP cathode notch structures.

A well established fabrication technique which uses cleaving and ultrasonic bonding has been used to evaluate the performance of new wafers. In addition, an integral heat sink (IHS) process is being developed which will improve the reliability of InP devices. InP IHS processing is especially difficult because of the incompatibility of the contact metallizations and the commonly used bromine-based mesa etchants.

During this reporting period, thirteen cathode notch wafers were evaluated. Noise figures of 8.5 dB with 6 dB gain have been achieved at the lower end of Ka-band. Noise figures below 7.5 dB with 4 dB gain have been measured in the upper end of Ka-band. Noise figures less than 9.0 dB with 6 dB of gain have been achieved at 45 GHz.

Four amplifier circuits are available for device evaluation in the 26.5 to 40.0 GHz range having nominal center frequencies of 29.5, 33.0, 37.0 and 38.0 GHz. Three circuits have been designed, fabricated and successfully tested in the 40.0 to 60.0 GHz range. Nominal center frequencies of these three circuits are 43.5, 50.0 and 56.5 GHz. All of these circuits are of the coaxial waveguide hybrid type. Six dB gain has been observed with these circuits over the entire 40-60 GHz band.

## 2. DEVICE DESIGN

### 2.1 THREE LAYER VERSUS CATHODE NOTCH

Two InP Gunn device structures are being employed in this program, a three layer structure and a cathode notch structure. The idealized doping profile of an InP three layer structure as well as a typical electric field profile are shown in Figure 2.1. The three layer structure consists of three epitaxial layers: a heavily doped  $n^+$  buffer layer; a lightly doped  $n$  active layer; and, a heavily doped  $n^+$  contact layer. The actual doping profile specifications of doping levels and layer thicknesses for operation in specific frequency intervals throughout Ka-band (26.5-40 GHz) and U-band (40-60 GHz) were reported previously [6].

The idealized doping profile of an InP cathode notch structure is shown in Figure 2.2 as well as a typical electric field profile. The cathode notch structure consists of four epitaxial layers: a heavily doped  $n^+$  buffer layer; an undoped  $n^-$  notch layer; a lightly doped  $n$  active layer; and, a heavily doped  $n^+$  contact layer. The actual doping profile specifications of doping levels and layer thicknesses were also reported previously [6].

The static electric field profile in a uniformly doped active region of a three layer device increases slowly from the cathode contact to a peak value near the anode if the injected space charge density is at all comparable to the fixed charge density in the active layer. Thus, the electric field is very non-uniform throughout the active region, and in fact is near threshold over a considerable fraction of the active layer. The generation of noise is greatest when the electric field is near threshold, due to the hot electron diffusion coefficient being maximized at threshold. Thus, a non-uniform field distribution with a long threshold-field transition region gives rise to excess noise. The results of calculations by Sitch and Robson [7] of the noise measure

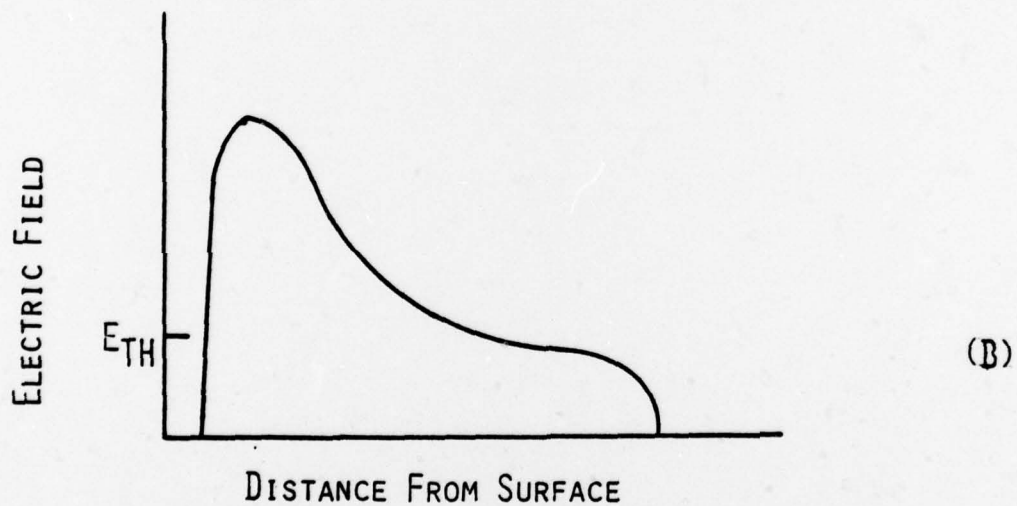
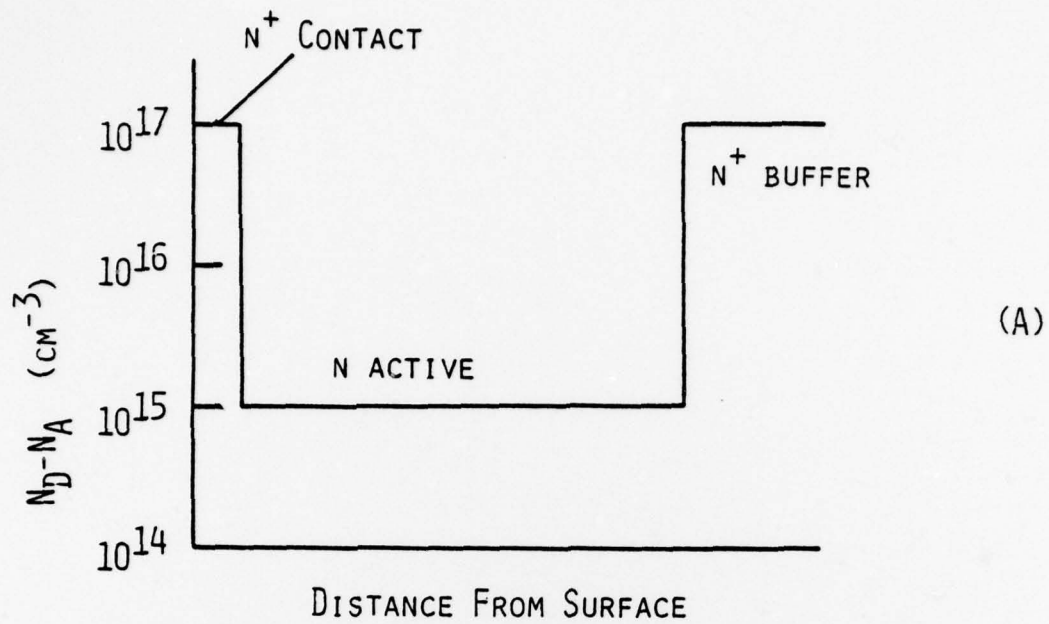


FIGURE 2.1 INP THREE LAYER STRUCTURE

(A) IDEALIZED DOPING PROFILE

(B) TYPICAL ELECTRIC FIELD DISTRIBUTION

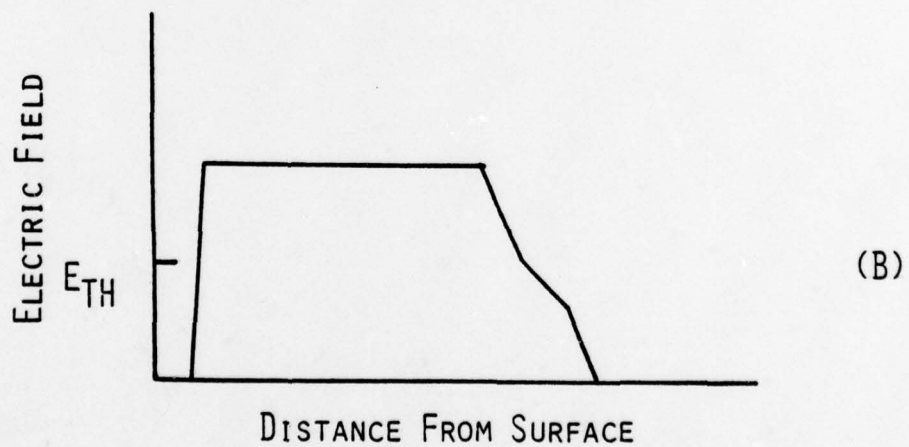
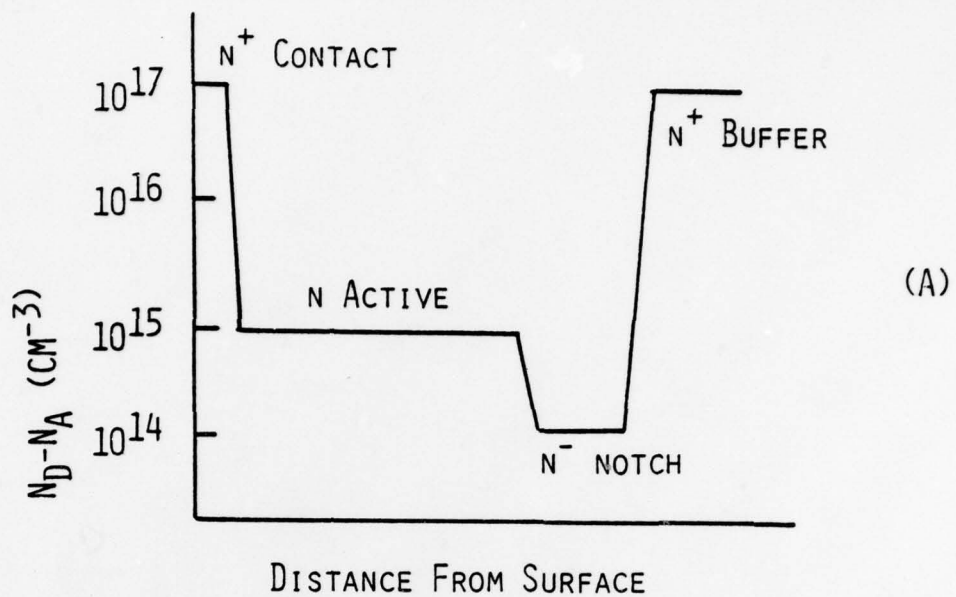


FIGURE 2.2 InP CATHODE NOTCH STRUCTURE

(A) IDEALIZED DOPING PROFILE

(B) TYPICAL ELECTRIC FIELD DISTRIBUTION

of three layer devices is reproduced in Figure 2.3 and shows a strong dependence on the  $nl$  product of the active layer.

As shown in Figure 2.2, the use of a low doping notch at the cathode can be used to produce a device with an electric field distribution which is uniform throughout the active region. The cathode notch region with its lower donor density drives the electric field above threshold in a very short distance. If the notch doping level and length are properly selected, the injected space charge at the downstream end of the notch can be forced to equal the fixed donor density, achieving space charge neutrality and uniform electric field across the active region. Curves in Figure 2.3 of Sitch and Robson show the dependence of the noise measure of an InP uniform field device for active layer field levels of 20, 30 and 40 kV/cm. An electric field of 20 kV/cm is optimum for low  $nl$  product devices, with minimum noise measure occurring for an  $nl$  product of  $5 \times 10^{10} \text{ cm}^{-2}$ .

## 2.2 Cathode Notch Parameters

The curves of Figure 2.4 illustrate the relationship between the notch doping level and length for various active layer doping levels which must be satisfied if a uniform field of 20 kV/cm is to be achieved in the active layer. These curves were generated using a computer program which calculates the spatial variations of the electric field and space charge density, the required notch length, and the voltage drops across the notch and active layers once a notch doping, an active layer doping and an active layer length are specified. For a given active layer doping, selection of the notch doping and length which fall on the corresponding curve will assure that the field builds up through the notch to 20 kV/cm at the downstream end and that space charge neutrality is satisfied, and therefore, that a uniform field will result in the active region. Notch design curves have been generated for active layer doping levels ranging from  $6 \times 10^{14} \text{ cm}^{-3}$  to  $2 \times 10^{15} \text{ cm}^{-3}$ .

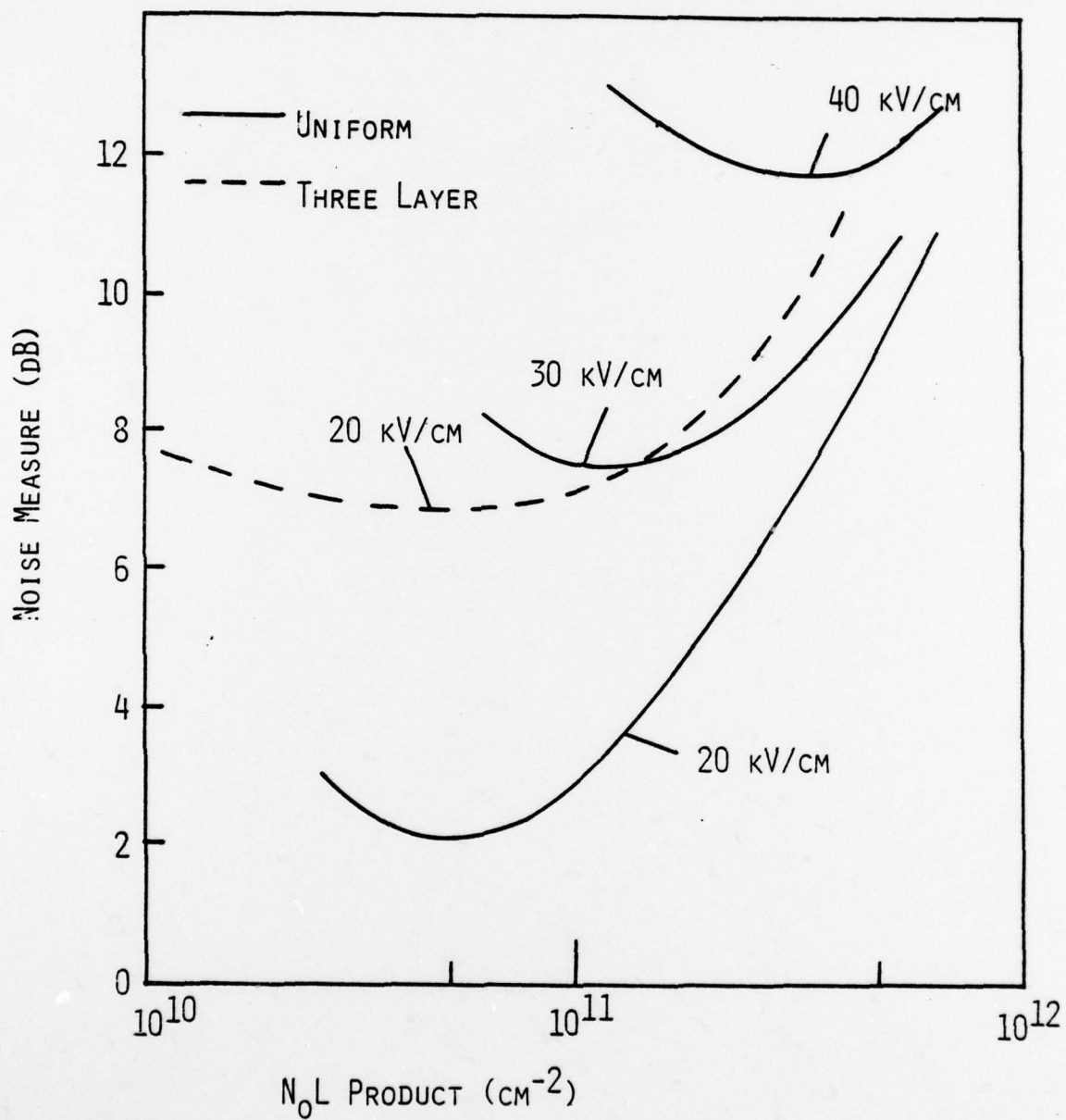


FIGURE 2.3. DEPENDENCE OF NOISE MEASURE ON ACTIVE LAYER  $N_0L$  PRODUCT FOR  $\text{InP}$

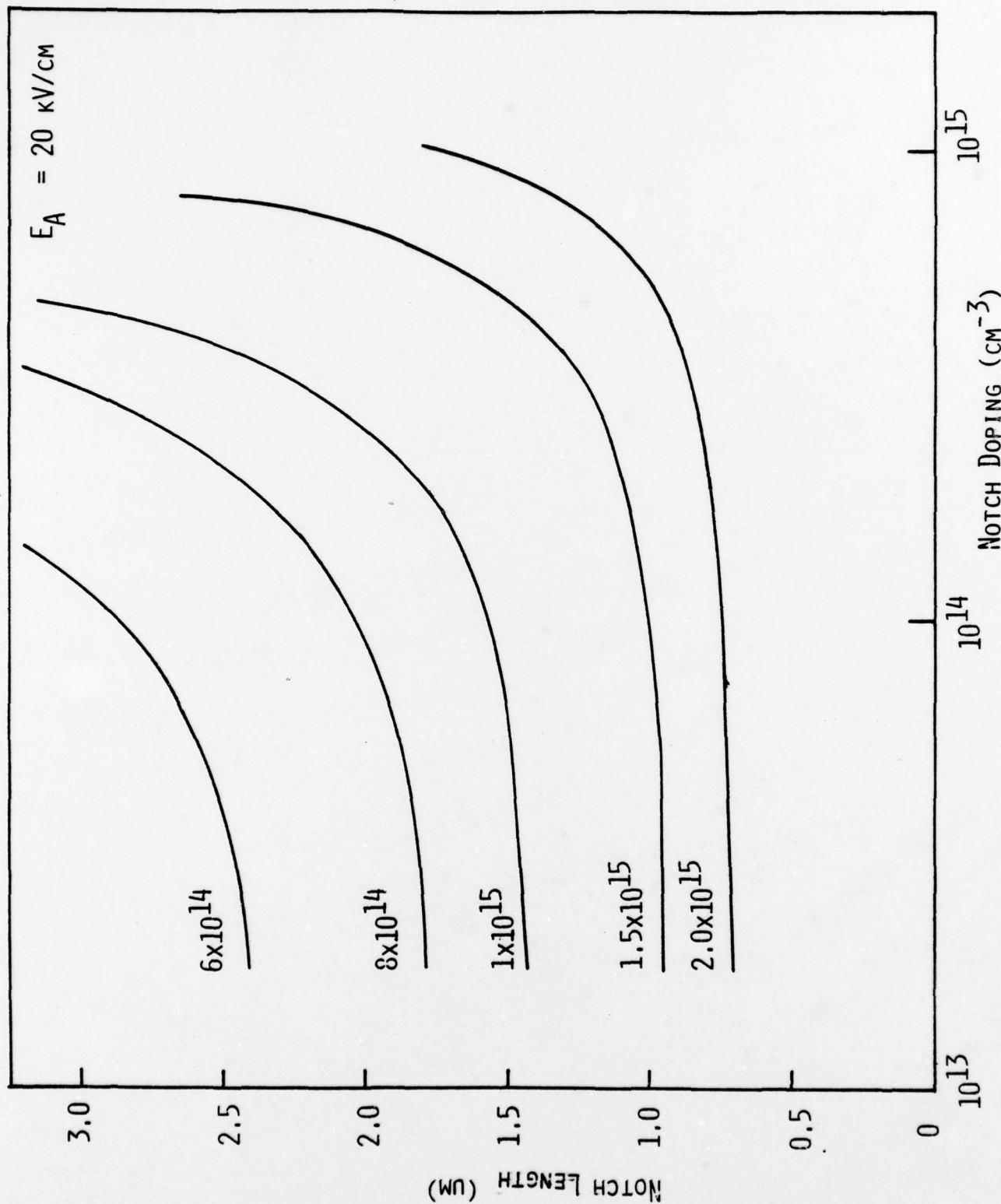


FIGURE 2.4 NOTCH DOPING VERSUS LENGTH FOR SPECIFIC ACTIVE DOPINGS

There are several important factors which must be taken into account in the selection of the profile parameters of a cathode notch device depending on the frequency of operation, the gain level and noise figures which are desired. Since a cathode notch device has a uniform electric field in the active layer, the length of this layer will be considerably shorter than that of a three layer device for the same frequency of operation. The  $nl$  product of the active layer should be as low as possible but not lower than  $5 \times 10^{10} \text{ cm}^{-2}$  to achieve low noise. However, a reduction in  $n$  for a given  $l$  results in lower gain as well. Therefore, in practice, a compromise must be made on the  $nl$  product in order to achieve low noise with a reasonable gain level. The notch parameters for a specific uniform field in the active layer are independent of the active layer length; they are dependent only on the active layer doping level. As the active layer doping is decreased in an effort to decrease the  $nl$  product of the active layer, the required notch length becomes greater. When this width becomes comparable to the active layer length, a significant resistance is added in series with the negative resistance of the active layer, effectively reducing the negative resistance of the device. This results in reduced gain. As the operation of the cathode notch device is pushed to higher frequencies (shorter active layer lengths) this effect becomes more significant and provides a fundamental limit to the lowest feasible  $nl$  product and therefore the lowest noise measure which is practical with this structure.

### 3. InP VAPOR PHASE EPITAXIAL GROWTH

For growth of device quality material, precise control of the growth rates and doping levels is needed. Maintenance of low carrier concentration for growth of notch profiles is also essential. Towards these ends, extensive work was done during this reporting period to improve the material growth process. The excessive wall deposits that were interfering with maintenance of a constant growth rate were considerably reduced by going to a slightly sloping temperature gradient in the deposition zone. Growth rates as a result, increased from a typical value of .07  $\mu\text{m}/\text{min.}$  to 0.14  $\mu\text{m}/\text{min.}$  At temperatures higher than 650°C, toward the upstream side, growth rates as high as 0.32  $\mu\text{m}/\text{min.}$  were obtained. Reduction in the wall deposits also improved the run to run reproducibility of the growth rates.

Excellent quality of the growth layers with mirror smooth surfaces is also being obtained by using InP substrates oriented  $2^\circ$  off (100) towards (110). These results have been obtained from two ingots. This allowed us to vary other VPE parameters over a wider range and still have good surface quality for device processing. Off orientation growth with the use of higher mole fraction  $\text{PCl}_3$  has yielded consistently low background carrier concentrations allowing low doped notch profiles. An increase in background doping, however, has been observed after several contact layer and buffer layer growths. This is possibly caused as a cumulative effect of back diffusion of  $\text{H}_2\text{S}$  to the source and can conceivably be reduced by some kind of baffle arrangement. This factor is not severe enough at present to warrant immediate attention. Reproducibility of active layer doping level is, however, still poor, since the ppm of  $\text{H}_2\text{S}$  needed to attain the required doping level of  $< 1 \times 10^{15}$  has been of the order of  $< 10^{-3}$

Thus, control of flows with the present dilution system has been difficult for low level flows. Therefore, a 5 liter mass flow controller for  $H_2$  dilution is being acquired to facilitate attainment of lower ppm of  $H_2S$ . The use of 50 ppm  $H_2S$  tank gas will also be considered.

The effect of In bakeout time has also been studied as to its effects on the notch doping level. Two hour initial bakeout is now being used as opposed to the 16 hour and 64 hour periods as longer bakeout times were found to increase doping levels, most likely because of silicon incorporation in the source from the boat and the reactor walls. Short bakeouts and high  $PCl_3$  mole fractions have been used to grow cathode notch material with the lowest notch doping levels yet measured. These results, combined with a significant improvement in growth rate control, allowed us to grow many cathode notch wafers suitable for device fabrication (see Table 3.1). Most of the notch doping levels were in the  $10^{13} \text{ cm}^{-3}$  range with a low of  $3.1 \times 10^{13} \text{ cm}^{-3}$ . Doping profiles for five of these runs are shown in Figures 3.1 through 3.5. The notch profiles show very clean transitions for buffer/notch and notch/active layer interfaces as well as reasonably flat active layer profiles except for SSW 53-7 (Figure 3.3) which drops rather sharply. Flat active layer doping as low as  $6 \times 10^{14} \text{ cm}^{-3}$  was obtained (Figure 3.1, SSW 53-5).

The effect of the high  $PCl_3$  mole fraction can be seen in the 53 series runs. Runs 53-4 through 53-7 grown with a high mole fraction ( $4 \times 10^{-2}$ ) had notch doping levels of  $3.1$ - $6.2 \times 10^{13} \text{ cm}^{-3}$  whereas run 53-2 with a lower mole fraction ( $9.23 \times 10^{-3}$ ) had a much higher notch doping of  $2.0 \times 10^{14} \text{ cm}^{-3}$ . In addition, background doping normally increases as a run series progresses yet these doping levels remained low. Series 54 had very low notch doping as well except for 54-3 at  $2.0 \times 10^{14} \text{ cm}^{-3}$ . However, 54-3 was a very narrow notch (1.0  $\mu\text{m}$ ) and would have been lower if it was as thick as the others.

TABLE 3.1  
VPE InP CATHODE NOTCH WAFERS\*

RUN NO. SSW	N <sup>+</sup> BUFFER		N <sup>-</sup> NOTCH		N ACTIVE		N <sup>+</sup> CONTACT		PCl <sub>3</sub> MOLE FRACTION
	N (cm <sup>-3</sup> )	T (μm)	N (cm <sup>-3</sup> )	T (μm)	N (cm <sup>-3</sup> )	T (μm)	N (cm <sup>-3</sup> )	T (μm)	
52-9	1.0e17	3.0	4.8e13	2.4	9.0e14	3.2	1.0e17	1.0	4.0x10 <sup>-2</sup>
53-2	2.1e17	2.9	2.0e14	1.7	2.5e15	3.9	2.1e17	1.0	9.23x10 <sup>-3</sup>
53-4	1.5e17	3.4	5.1e13	1.7	1.4e15	4.6	1.5e17	1.0	4.0x10 <sup>-2</sup>
53-5	1.3e17	3.5	3.2e13	2.5	6.0e14	3.9	1.3e17	1.3	4.0x10 <sup>-2</sup>
53-6	1.4e17	3.8	3.1e13	2.8	1.0e15	2.1	1.4e17	1.5	4.0x10 <sup>-2</sup>
53-7	1.7e17	3.3	6.2e13	1.7	8.2e14	2.3	1.7e17	1.0	4.0x10 <sup>-2</sup>
54-3	1.4e17	3.4	2.0e14	1.0	9.4e14	0.7	1.4e17	0.9	4.0x10 <sup>-2</sup>
54-5	1.3e17	3.0	5.6e13	1.8	1.2e15	1.8	1.3e17	1.1	4.0x10 <sup>-2</sup>
54-7	1.6e17	2.9	7.7e13	1.5	1.8e15	1.7	1.6e17	1.3	4.0x10 <sup>-2</sup>
54-8	1.5e17	3.6	1.1e14	1.6	1.1e15	1.7 <sup>M</sup> 1.3 <sup>E</sup>	1.5e17	1.3	4.0x10 <sup>-2</sup>

\* Measurements at 77°K

+ Mole Fraction for Undoped Notch Layer. The mole fraction is slightly lower for doped layers where additional H<sub>2</sub>S/H<sub>2</sub> is added to the reactor thereby causing PCl<sub>3</sub> dilution.

† 1.7 μm is the metallurgical thickness, 1.3 μm is the electrical profile thickness.  
(see text for explanation)

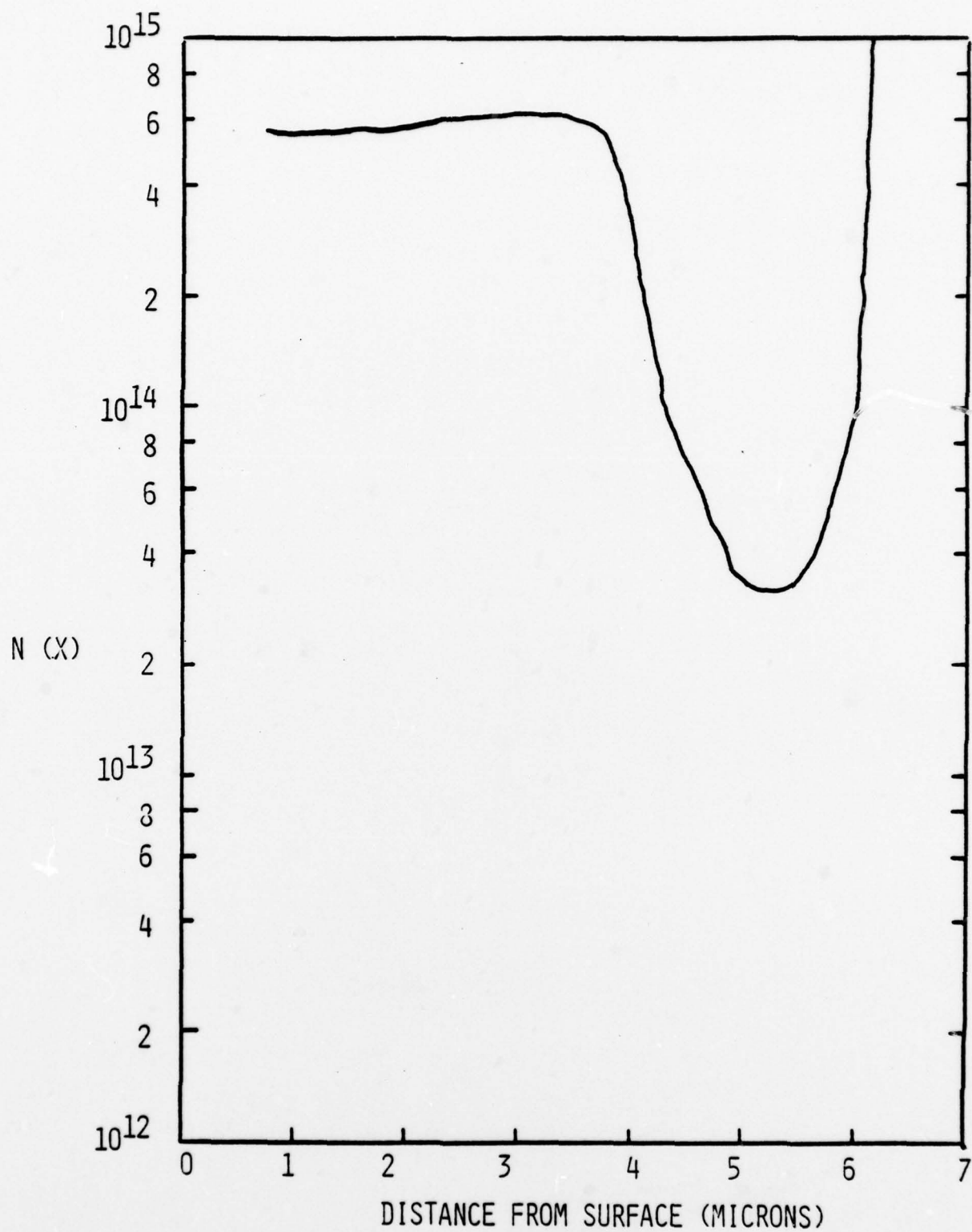


FIGURE 3.1 INP VPE SSW53-5T<sub>1</sub>

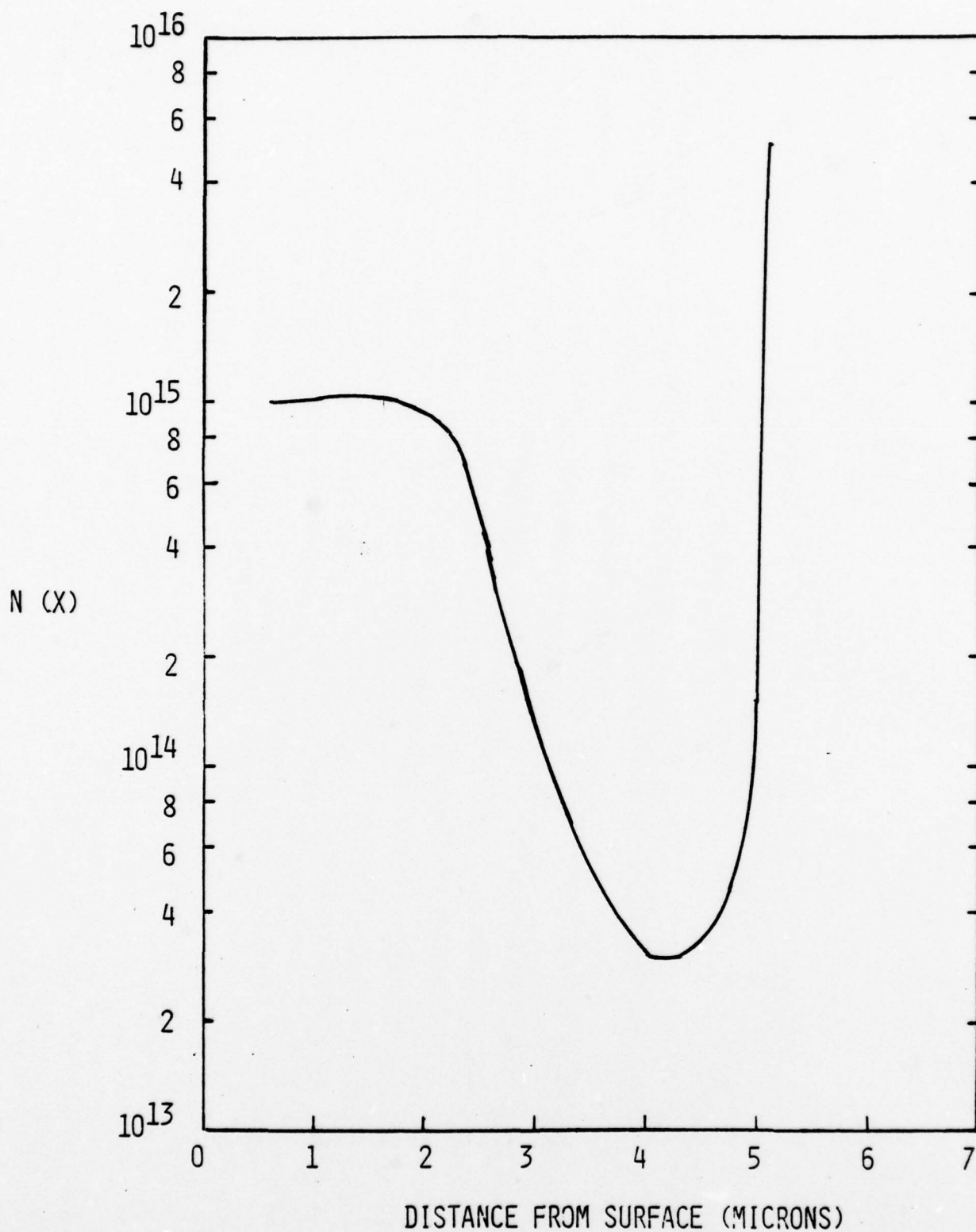


FIGURE 3.2 INP VPE SSW 53-6T<sub>1</sub>

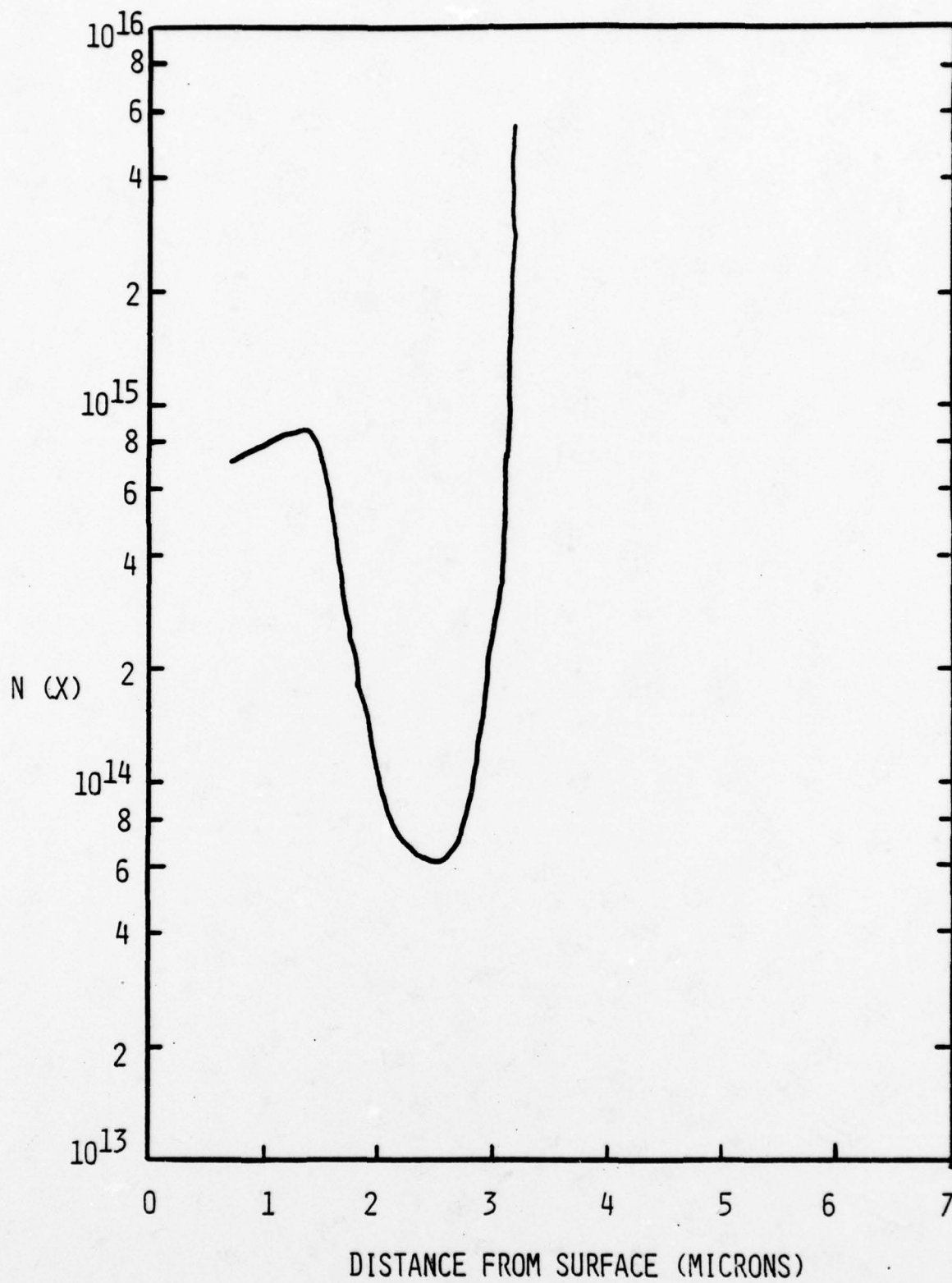


FIGURE 3.3. INP VPE SSW 53-7T<sub>1</sub>

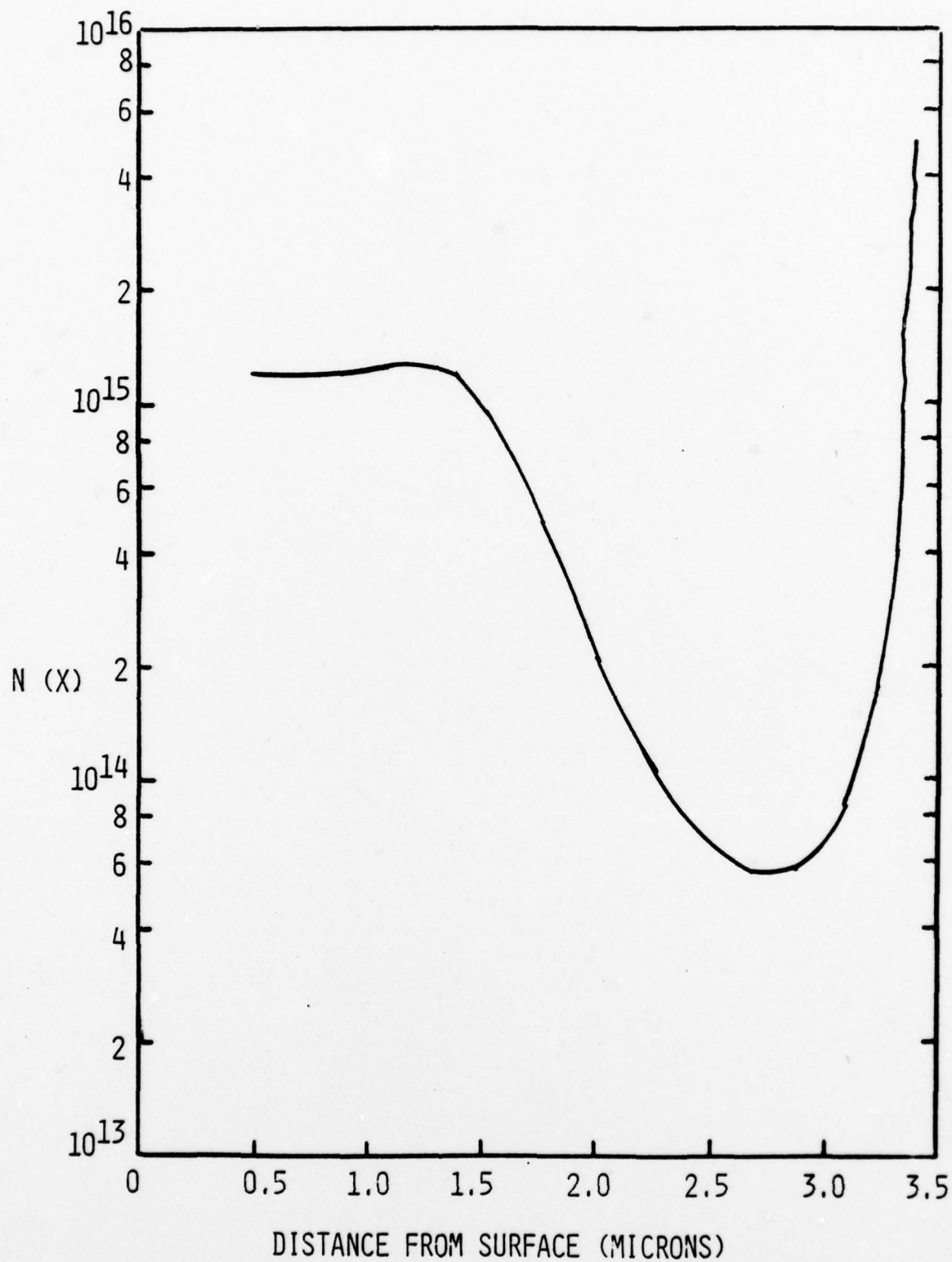


FIGURE 3.4. INP VPE SSW .54-5T<sub>1</sub>

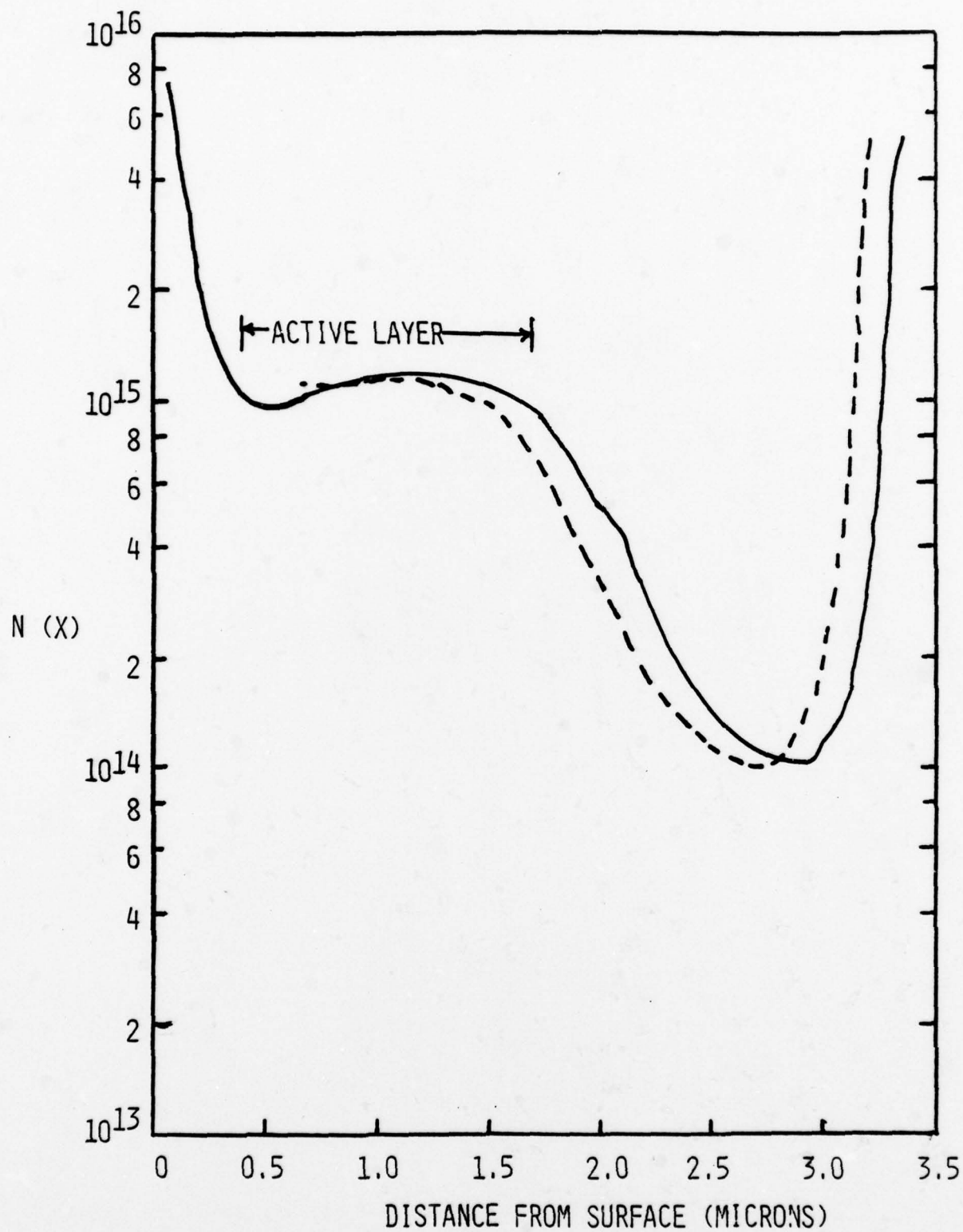


FIGURE 3.5.  $\text{InP VPE SSW 54-8T}_1$

It is interesting to note that run 52-9 had a low doped notch of  $4.8 \times 10^{13} \text{ cm}^{-3}$ . It was grown with a high mole fraction but the indium source had a 16 hour bakeout compared to a 2 hour bakeout in series 53 and 54. However, it was also grown upstream of the  $\text{H}_2\text{S}$  doping inlet. This demonstrates the possible use of this growth technique if required in future runs to maintain or lower notch doping levels.

Two thicknesses are given for the active layer thickness of wafer 54-8 in Table 3.1. Notch thicknesses are obtained directly from doping profiles but the complete active layer thickness is generally not available from the profile because part of it is removed when removing the contact layer. Therefore, the active layer thickness is obtained by subtracting the notch thickness from the sum of the notch and active thickness as obtained from a metallurgical section. This is referred to as the metallurgical thickness (M). However, in removing the contact layer of 54-8 the contact/active interface was obtained along with a complete active-notch profile as shown in Figure 3.5. The electrical thickness (E) given in Table 3.1 is obtained directly from this profile. For comparison, the metallurgical thickness is also given. The actual active layer thickness operational in the Gunn diode may fall in between these two values.

An important question is whether the low doping obtained with short 2 hour indium bakeout times is due to high purity material or compensated material. Table 3.2 gives Hall and C-V data for mobility evaluation runs in series 52-54. Both series 52 and 54 with 16 hour and 2 hour bakeout times show normal high purity results. Series 54 also gave high purity results for both high and low  $\text{PCl}_3$  mole fractions. Series 53 behaved differently and sample 53-1 showed carrier concentration freeze-out from room temperature to  $77^\circ\text{K}$  as well as low mobility data indicating compensation. By run 53-8, freeze-out did not occur but mobility remained low. Both of these runs used a low  $\text{PCl}_3$  mole fraction ( $9.08 \times 10^{-3}$ ). However, most of the device runs in series 53 were grown with a high  $\text{PCl}_3$  mole fraction (see Table 3.1) and run 53-9 gave good high purity mobility

TABLE 3.2  
VPE INP HALL SAMPLES, C-V DATA

RUN NO.	In BAKEOUT (hours)	PCl <sub>3</sub> MOLE FRACTION	C-V, 77°K		N <sub>D</sub> -N <sub>A</sub> cm <sup>-3</sup>		HALL DATA		$\mu_H$ , cm <sup>2</sup> /v-sec 77°K
			(N <sub>D</sub> -N <sub>A</sub> ) cm <sup>-3</sup>	Room Temp	Room Temp	77°K	Room Temp	77°K	
52-1	16	9.08x10 <sup>-3</sup>	7.6e14	1.2e15	1.1e15	4460	57,430		
53-1	2	9.08x10 <sup>-3</sup>	4.2e15	1.5e16	4.5e15	2330	18,870		
53-8	2	9.08x10 <sup>-3</sup>	5.4e15	9.0e15	7.6e15	2857	18,267		
53-9	2	3.81x10 <sup>-2</sup>	3.1e15	3.7e15	3.1e15	3966	27,496		
54-1	2	9.08x10 <sup>-3</sup>	1.4e15	5.7e14	4.8e14	4262	40,768		
54-2	2	3.74x10 <sup>-2</sup>	1.2e15	1.6e15	1.3e15	4458	47,799		

without carrier freeze out when the high mole fraction was used. Device performance from these wafers is also consistent with high purity material and stable doping profiles.

We now have enough runs with the new furnace temperature profile to show that a significant improvement in growth rate reproducibility has been obtained in addition to fewer wall deposits and a growth rate increase. Table 3.3 gives growth rate data from three run series with the old profile. Standard deviations range from  $\pm 20\%$  to  $\pm 47.5\%$  with an average of  $\pm 35.3\%$ . As shown in Table 3.4, standard deviations range from 4.1% to 7.9% (average  $\pm 5.8\%$ ) with the new profile. In addition, the average growth rate is 2.2 times greater with the new profile. Growth rates are given separately for buffer layers and either active or notch plus active layers. This is done because the growth rate is faster for initial growth when InP wall deposits are small. As a run progresses, wall deposits build up and the growth rate on the wafer slows down because more deposition occurs on wall deposits. It is of interest that the average ratios of the buffer to active/notch growth rate is only 1.18 for the new profile whereas it is 1.59 for the old profile. The new profile significantly reduces wall deposits and hence gives a more uniform growth rate for the entire epitaxial structure.

Four cathode notch runs were made with the source from growth series SSW54. One of them with the parameters listed in Table 3.5 was used for device fabrication. This run (54-9) was made in the conventional manner with the substrate behind the  $H_2S$  doping inlet. For the other three runs in this series SSW54-10, 54-11 and 54-12, the substrate was kept ahead of the  $H_2S$  inlet during notch and active layer growth, the doping being achieved by back diffusion. Higher flow rates of  $H_2S$  mixture could be used in this situation allowing better flow control. The results for the three growth runs are shown in Table 3.6.

TABLE 3.3

VPE InP GROWTH RATES\* - OLD FURNACE PROFILE

RUN NO.	EPI LAYER GROWTH RATE ( $\mu\text{m}/\text{min}$ )		
	NOTCH AND ACTIVE	ACTIVE	BUFFER
48-1	.059		.101
48-2	.042		.066
48-3	.072		.123
48-4	.035		.063
48-5	.027		.034
AVE	.047		.077
$\sigma$	$\pm .018$ ( $\pm 38.3\%$ )		$\pm .035$ ( $\pm 45.5\%$ )
49-4		.065	.101
49-5		.041	.055
49-6		.049	.078
49-7		.046	.071
AVE		.050	.076
$\sigma$		$\pm .010$ ( $\pm 20.0\%$ )	$\pm .019$ ( $\pm 25.0\%$ )
50-1			.086
50-2			.071
50-4			.127
50-5			.036
AVE			.080
$\sigma$			$\pm .038$ ( $\pm 47.5\%$ )

\*  $\text{PCl}_3$  mole fraction was  $9.23 \times 10^{-3}$  during notch growth  
 Ratio of (buffer/notch and active) growth rate = 1.59

TABLE 3.4

VPE InP GROWTH RATES\* - NEW FURNACE PROFILE

SSW RUN NO.	EPI LAYER GROWTH RATE ( $\mu\text{m}/\text{min}$ )	
	NOTCH AND ACTIVE	BUFFER
53-3	.135	.160
53-4	.134	.163
53-5	.137	.165
53-6	.148	.180
53-7	.141	.157
AVE	.139	.165
$\sigma$	$\pm .0057$ ( $\pm 4.1\%$ )	$\pm .0089$ ( $\pm 5.4\%$ )
54-3	.121	.160
54-4	.140	.140
54-5	.123	.143
54-6	.136	.157
54-7	.125	.138
54-8	.136	.170
54-9	.129	.152
AVE	.130	.151
$\sigma$	$\pm .0074$ ( $\pm 5.7\%$ )	$\pm .012$ ( $\pm 7.9\%$ )

\*  $\text{PCl}_3$  mole fraction was  $4.0 \times 10^{-2}$  during notch growth  
 Ratio of (buffer/notch and active) growth rate = 1.18

WAFER (SSW 54-9)

	Buffer $n^+$	Notch $n^-$	Active $n$	Contact $n^+$
$N_D - N_A$	$1.6 \times 10^{17}$	$5.7 \times 10^{13}$	$3.4 \times 10^{14}$	$1.6 \times 10^{17}$
T ( $\mu m$ )	3.2	1.8	2.4	1.3

TABLE 3.5

NOTCH WAFER FROM SERIES SSW54 DOPED IN CONVENTIONAL MANNER

SSW Run #	Notch $n^-$		Active Layer $n$		Initial Flow $H_2S$	ppm $H_2S$
	$N_D - N_A$	T ( $\mu m$ )	$N_D - N_A$	T ( $\mu m$ )	cc/min	
54-10	$2.1 \times 10^{14}$	1.6	$2.2 \times 10^{15}$	5.2	8.1	$5.98 \times 10^{-2}$
54-11	$1 \times 10^{14}$	1.3	$4.5 \times 10^{14}$	3.5	2.7	$2.01 \times 10^{-2}$
54-12	$2.4 \times 10^{13}$	3.1	$5 \times 10^{15}$	1.5	3.7	$2.75 \times 10^{-2}$

TABLE 3.6

NOTCH WAFERS FROM SERIES SSW54 DOPED BY BACK DIFFUSION

	Notch $n^-$		Active $n$		Contact $n^+$	
RUN #	$N_D - N_A$	T ( $\mu m$ )	$N_D - N_A$	T ( $\mu m$ )	$N_D - N_A$	T ( $\mu m$ )
SSW 55-5	$5.7 \times 10^{13}$	2.4	$1.7 \times 10^{15}$	3.81	$7.8 \times 10^{16}$	0.64
SSW55-6	$6 \times 10^{13}$	2.5	$5.5 \times 10^{16}$	1.80	$1.4 \times 10^{18}$	0.60

TABLE 3.7

NOTCH WAFERS GROWN WITHOUT  $N^+$  BUFFER LAYER

As these results show, it was difficult to control the active layer doping with this procedure. Since there was no significant improvement in the notch doping level, this procedure has now been discontinued in favor of the conventional growth process with the wafer behind the doping inlet.

Two more cathode notch structures were made with growth of the notch directly on an  $n^+$  Sn-doped substrate. Table 3.7 shows the doping level and thickness of various layers as derived from the C-V data and cleave and stain. The object of these two growth experiments without the buffer layer was to check the effect, if any, of residual  $H_2S$  after  $n^+$  layer growth on the background doping and subsequently on the active layer doping. However, no appreciable difference was observed in notch doping or the active doping of these two growths and those grown with an  $n^+$  buffer layer. It is also of interest to compare device performance of the two structures, with and without the buffer layer.

Following these runs, the system was dismantled, cleaned and leak checked again. A fresh indium source was added and the  $PCl_3$  bubbler refilled. Evaluation runs made after reactor cleaning indicate that previous background conditions have been fairly well re-established for further growth which will continue next month.

## 4. DEVICE FABRICATION

### 4.1 Scribe and Cleave Process

InP Gunn devices have been fabricated using two different techniques: a) scribe and cleave process; or, b) integral heat sink process. Most of the devices fabricated to date have been processed using the scribe and cleave method which has been discussed previously [6]. The main disadvantage of this process is the damage incurred by the chip in the scribing, cleaving and bonding processes. An in-package etch is used to remove the damage at the outer edges of the chip. This processing technique is also characterized by variation from diode to diode of the packaged device thermal resistance.

### 4.2 Integral Heat Sink Process

In the integral heat sink process (IHS), discrete heat sinks are plated directly onto the epi-layer side of the wafer. Device geometries are defined by photolithography and chemical etching. The IHS device is then soldered into the desired package. The result is a damage-free chip with a slightly higher but more reproducible thermal resistance.

The IHS process requires formation of device geometries by chemical etching. The most commonly used isotropic etchants for InP are bromine-based solutions. However, these etchants are not compatible with gold heat sinks and Au-Ge contact metallizations which are used with InP devices. The use of a bromine-based etchant requires special precautions to protect metallizations, such as using a buried contact or etchant resistant barrier layers (Ti, Pt) to protect the gold [6]. These techniques significantly increase the complexity of the device fabrication process and lower the yield.

To circumvent some of these problems, several new mesa etchants have been investigated. The most promising etchant investigated to date uses an  $\text{FeCl}_3$  and  $\text{H}_2\text{O}$  solution plus illumination [8]. The photogeneration of carriers increases the etch rate, causing illuminated areas to etch faster than unilluminated areas. It was found that the  $\text{FeCl}_3$  concentration has a significant effect on the roughness of the mesa walls and the formation of a film which inhibits the etching process eventually bringing it to a halt. Proper adjustment of the  $\text{FeCl}_3$  concentration can prevent the formation of this inhibiting film and results in mesas with acceptable wall roughness.

Figure 4.1 is an SEM photograph of a mesa which was etched using this process. A 125-micron, Au contact pad was used as a protective shadow mask during the etching of this 50 micron thick wafer. The mesa walls are much steeper than can be achieved with an isotropic etch and exhibit only a small amount of undercutting of the protective mask. The wall roughness was sufficiently small that a polishing etch was not required.

#### 4.3 Pedestal Mounted Diodes

A packaging scheme for devices to be used in microstrip circuits is being developed. Reliable operation of an InP Gunn device requires good heat sinking. For a microstrip application, it would be desirable to have a packaging scheme where the device can be inserted into the circuit with as little labor as possible, e.g. threading of bond wires through a very small hole in the microstrip is unacceptable. In addition, diodes should be easily replaceable.

Figure 4.2 is a photograph of an InP Gunn device which has been assembled for microstrip applications. The assembly process is outlined below:

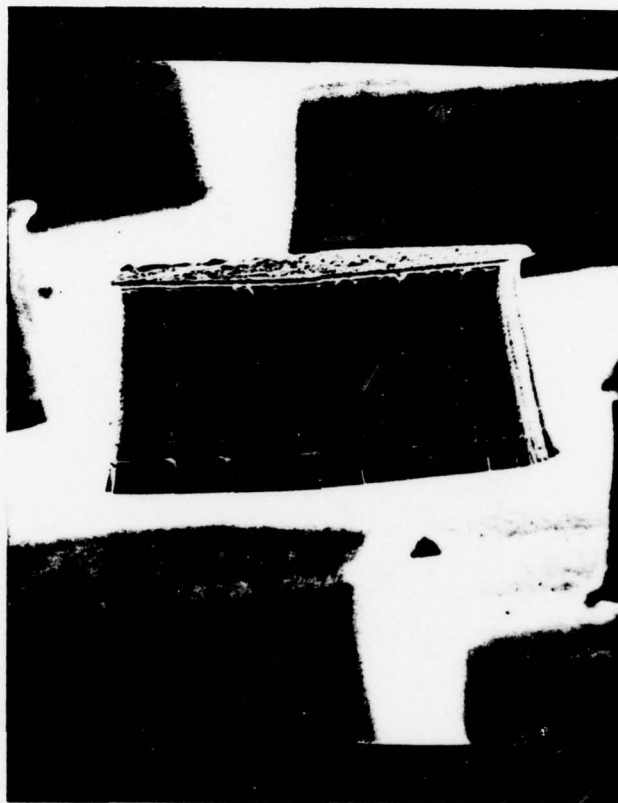


FIGURE 4.1. INP MESAS ETCHED USING  $\text{FeCl}_3$  PHOTORESISTIVE ETCHANT

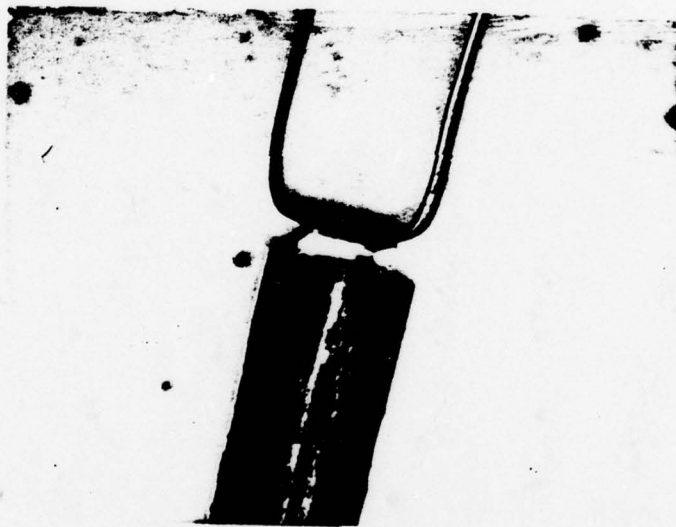


FIGURE 4.2. InP GUNN DEVICE MOUNTED ON A .010" DIAMETER  
STUD FOR MICROSTRIP APPLICATION

1. Cut OFHC copper wire (.010" diameter) and polish both ends until a .050" long stud is formed.
2. Au plate .010" x .050" copper stud.
3. Ultrasonically bond .0045" x .0045" InP scribe and cleave chip to one end of copper stud.
4. TC bond ribbon for top contact.
5. Apply small amount of resin to chip and ribbon to provide mechanical support to ribbon-chip bond.

The stud package of Figure 4.2 can be inserted through a .010" hole in a microstrip substrate into a .010" hole in a heatsink underneath the ground plane. The depth of the hole in the heatsink can be used to determine the vertical position of the diode in the microstrip circuit. Securing the stud in the heatsink can be accomplished by using low temperature solder, a set screw, or a variety of clamping assemblies. Ease of replacement may have to be traded for lower thermal resistance in selecting the best method of securing the stud.

Devices from EE120, a low doped cathode notch wafer have successfully been operated CW with this packaging scheme. Testing was limited to DC evaluation. The thermal resistance of several of these pedestal mounted diodes was measured using a liquid crystal technique. In order to perform these measurements, four pedestals were mounted in the center of the flange on an N-33 package as shown in Figure 4.3. Holes of .040" or .030" depth were drilled in the centers of N-33 packages and pedestals with diodes attached were soldered into these holes. Bond wires from the diodes were attached to quartz standoffs for bias connection. In addition, a chip from EE120 was bonded into an N-33 package without a pedestal. The result was five diodes with effective pedestal heights,  $H$ , of either .010" or .020".

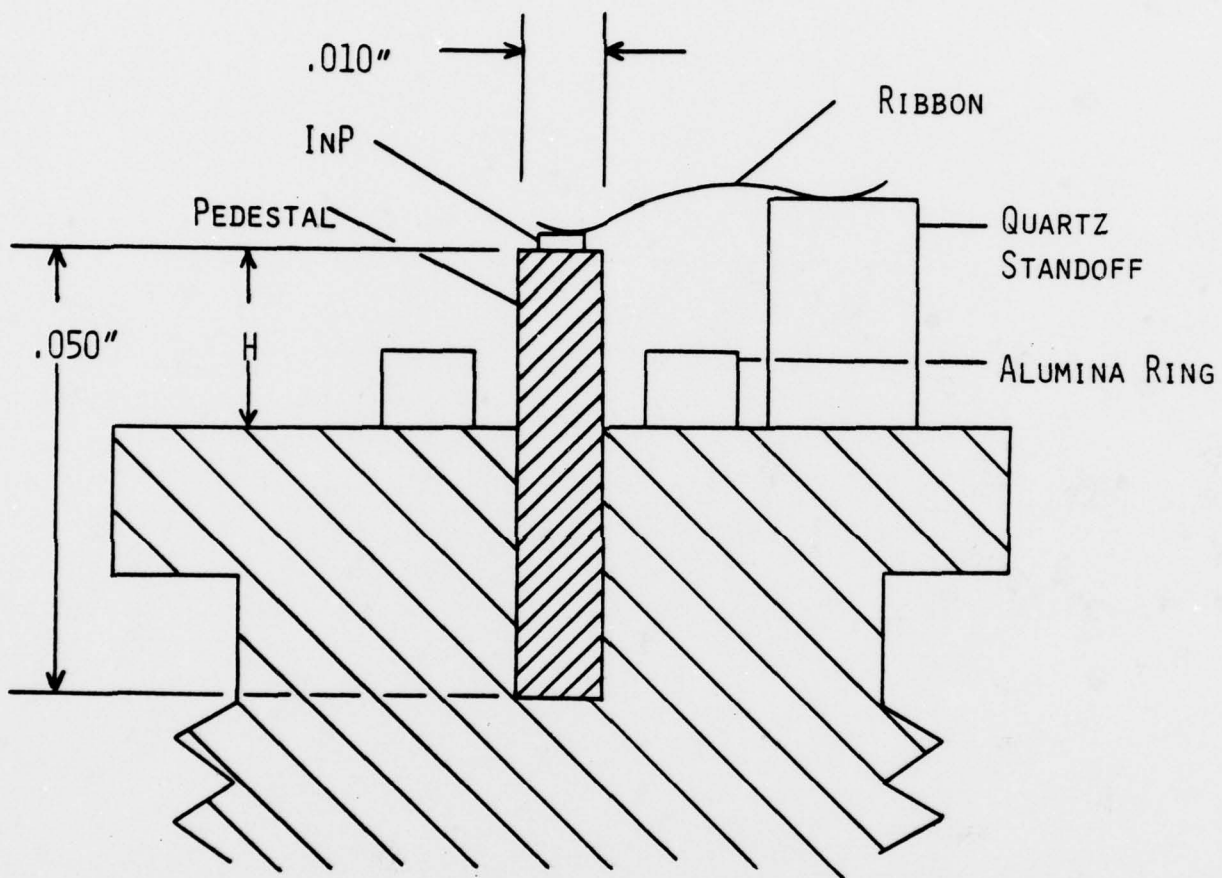


FIGURE 4.3. PACKAGE ASSEMBLY USED TO MEASURE THERMAL RESISTANCE OF PEDESTAL MOUNTED DIODES

A drop of liquid crystal having a transition temperature of  $122^{\circ}\text{C}$  was applied to the InP chip. While observing the surface of the chip through crossed polarizers of a microscope, the bias was increased until the liquid crystal film changed phase. The temperature of the heat sink was monitored with a thermocouple. The temperature drop from the chip to the heat sink was readily determined for specific bias conditions, thus giving a measure of the thermal resistance of the packaged device.

Table 4.1 lists the values of thermal resistance measured on five diodes using this technique. The pedestal mounted diodes have a thermal resistance which is 2.5 to 3.7 times greater than a standard packaged device. The pedestal height does not appear to be the limiting factor in the thermal resistance. Such high thermal resistances and large fluctuations from diode to diode probably result from a poor quality and non-reproducible ultrasonic bond of the chip to the .010" diameter pedestal. This is caused by several factors: a) surface roughness on the end of pedestal; b) movement and flexing of the pedestal in holder while bonding; and c) non-uniform pressure at chip-pedestal interface due to non-parallel alignment of surfaces of pedestal, chip and bonding tip. All of these factors can be eliminated in the future by using an IHS chip which is then soldered to the end of the pedestal.

DEVICE EE120	PEDESTAL HEIGHT (in)	CURRENT @ Neg 13 V (Amps)	THERMAL RESISTANCE (°C/Watt)
-3	0	.18	23
-4	.010	.18	75
-5	.010	.22	59
-6	.020	.18	85
-7	.020	.18	62

TABLE 4.1

THERMAL RESISTANCE OF PEDESTAL MOUNTED DIODES

## 5. RF EVALUATION

### 5.1 AMPLIFIER CIRCUITS

The RF performance of diodes from each new wafer was evaluated using several coaxial-waveguide amplifier circuits. The amplifier circuit shown in Figure 5.1 and described previously [6] consists of a coaxial line terminated on one end by the InP Gunn device and on the other end by a multisection low pass filter for DC bias insertion. A portion of the outer coax conductor is cut away and forms a reduced-height section of waveguide. This feature provides both a coax-to-waveguide transformation and an impedance transformation to full-height output waveguide. Circuit optimization for individual devices is accomplished by varying the center conductor length and/or diameter and by varying the recess of the diode package in the copper heat sink.

This circuit has been frequency scaled to provide circuits which will cover Ka-band (26.5-40 GHz) and U-band (40-60 GHz). In Ka-band, circuits with nominal center frequencies of 29.5, 33.0, 37.0 and 38.0 GHz are available for testing purposes. The performance of the 29.5 and 37.0 GHz circuits are being emphasized for use in staggered gain full band amplifiers. Figures 5.2 and 5.3 illustrate typical gain responses of the 29.5 and 37.0 GHz circuits, respectively. These two circuits nearly provide full band coverage. In U-band, three circuits with nominal center frequencies of 43.5, 50.0 and 56.5 GHz have been constructed. Figure 5.4 illustrates typical gain responses of these three circuits, and shows that they can be used to provide good gain coverage over the entire band. Of course, the gain, bandwidth and noise figures achieved with these circuits are strongly dependent on the structure of the particular device being used in the circuit.

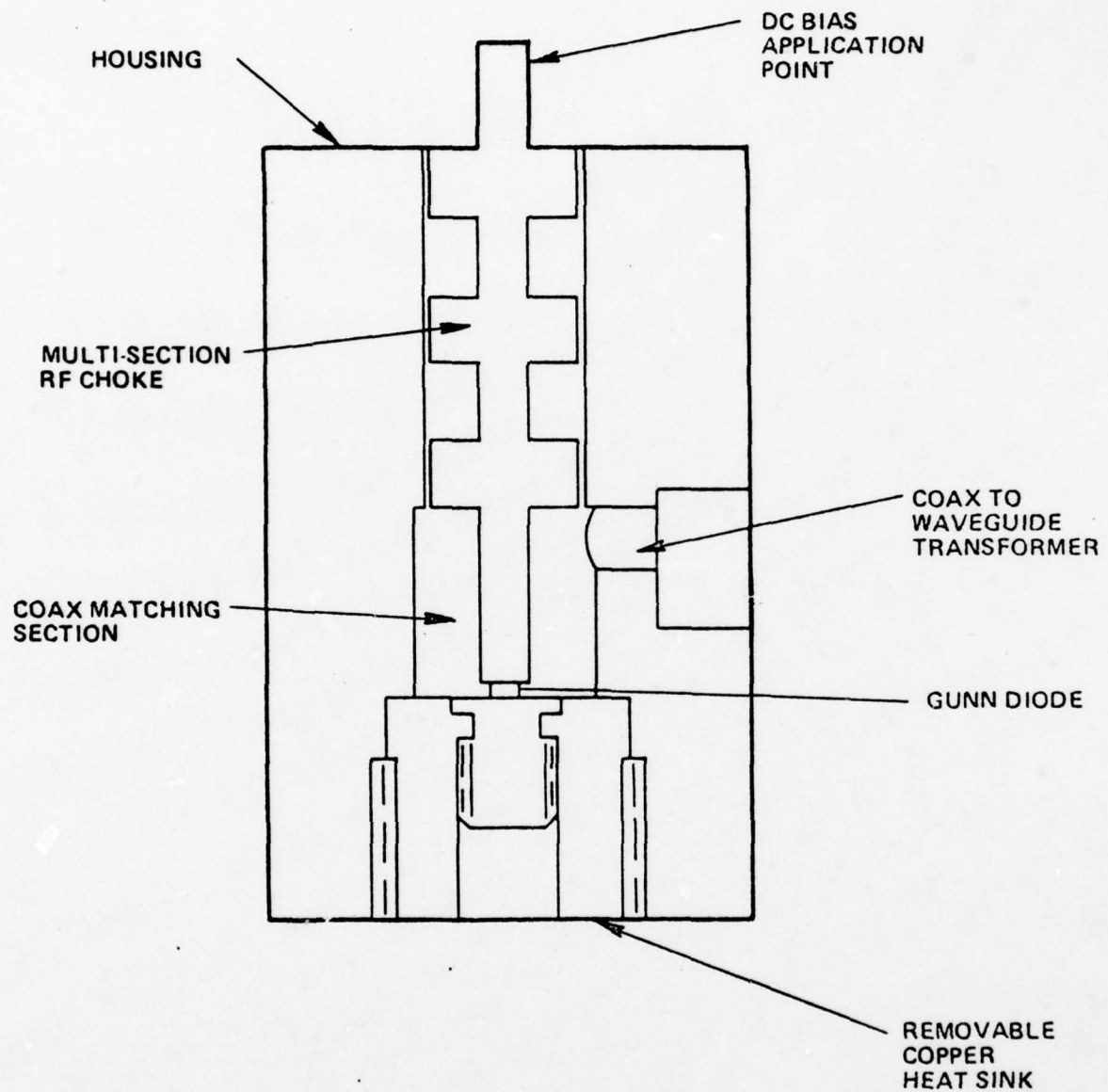


FIGURE 5.1. COAXIAL WAVEGUIDE HYBRID AMPLIFIER CIRCUIT

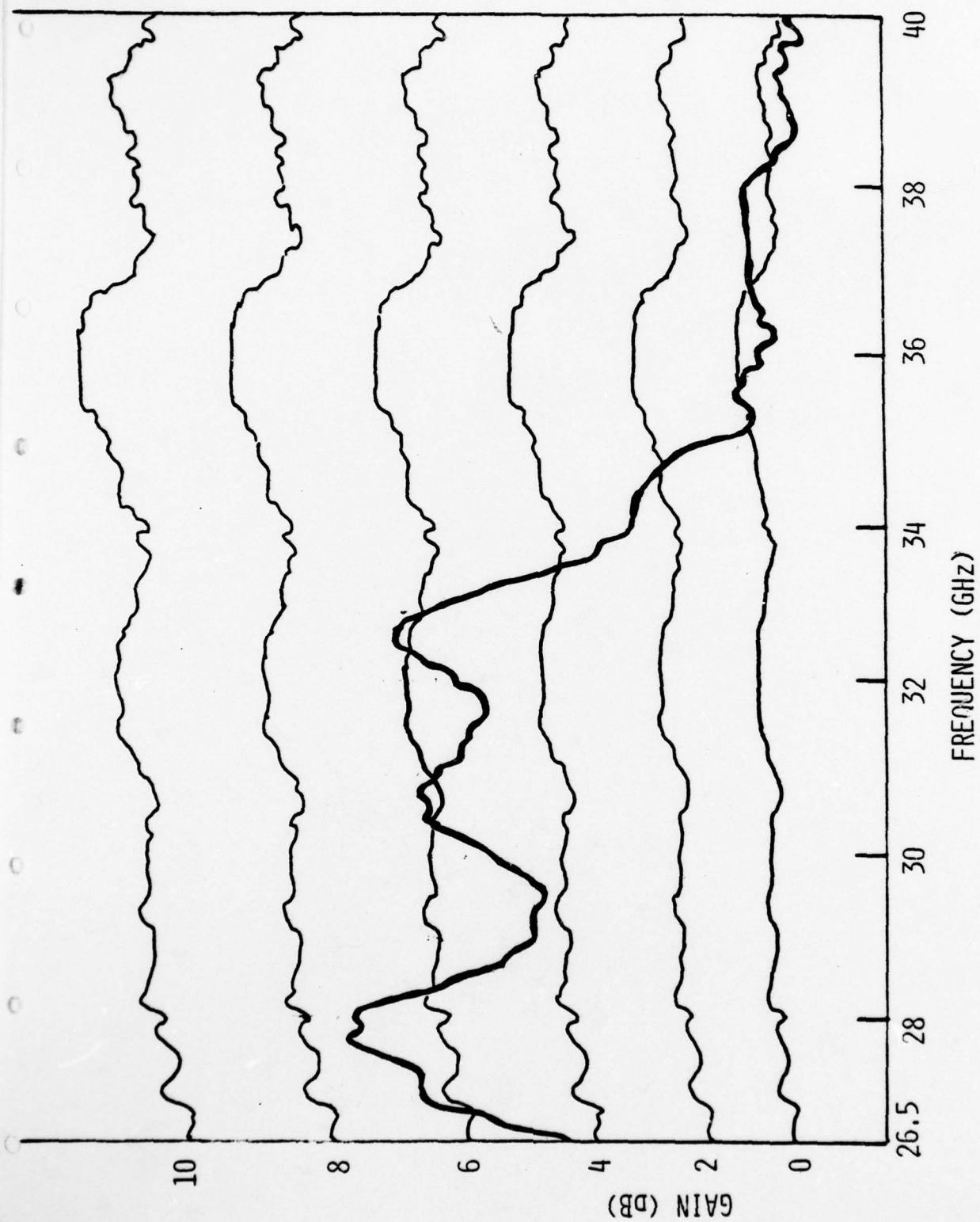


FIGURE 5.2 GAIN RESPONSE OF EE116 IN 29.5 GHz COAXIAL WAVEGUIDE CIRCUIT

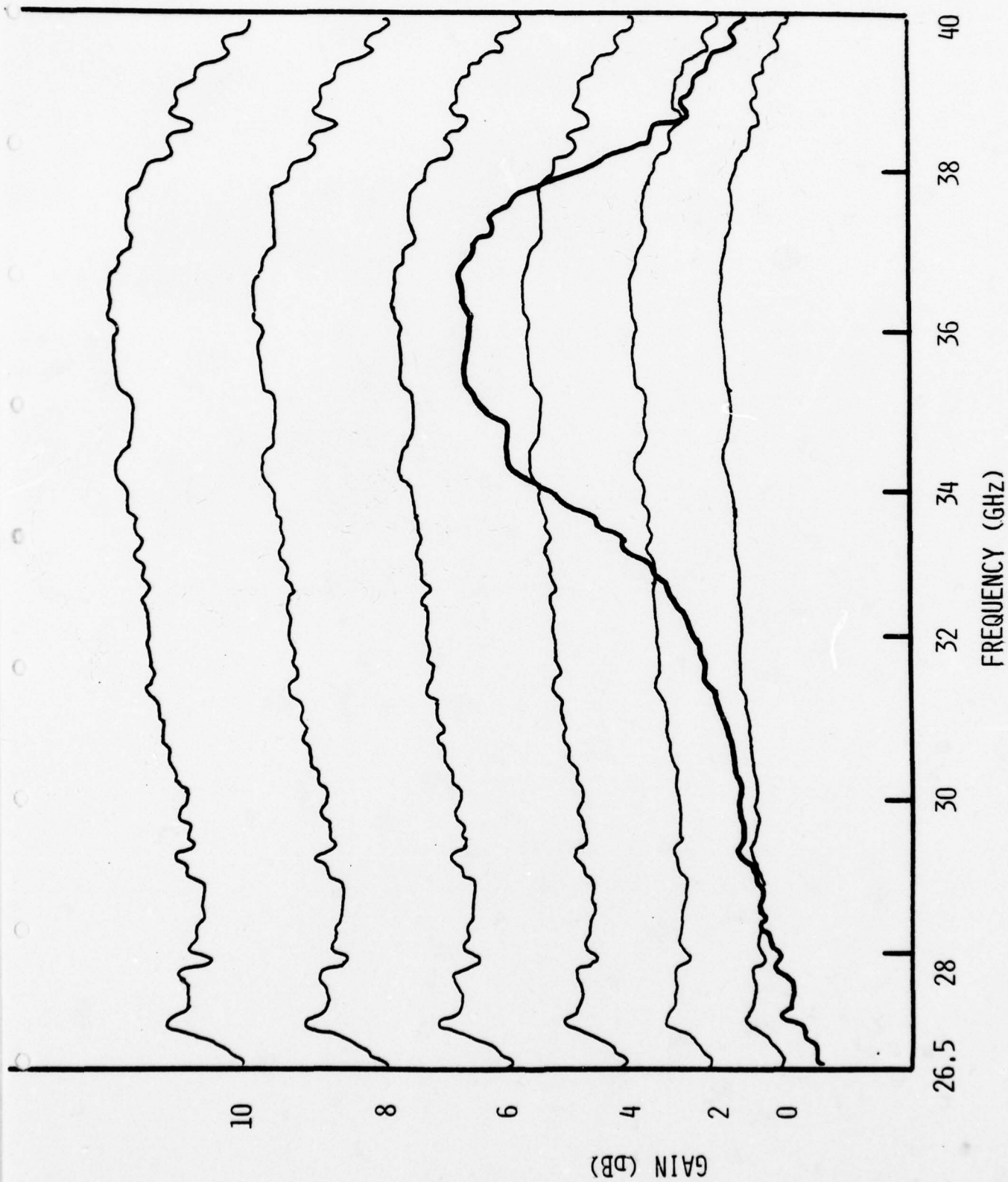


FIGURE 5.3. GAIN RESPONSE OF EE125 IN 37.0 GHz COAXIAL WAVEGUIDE CIRCUIT

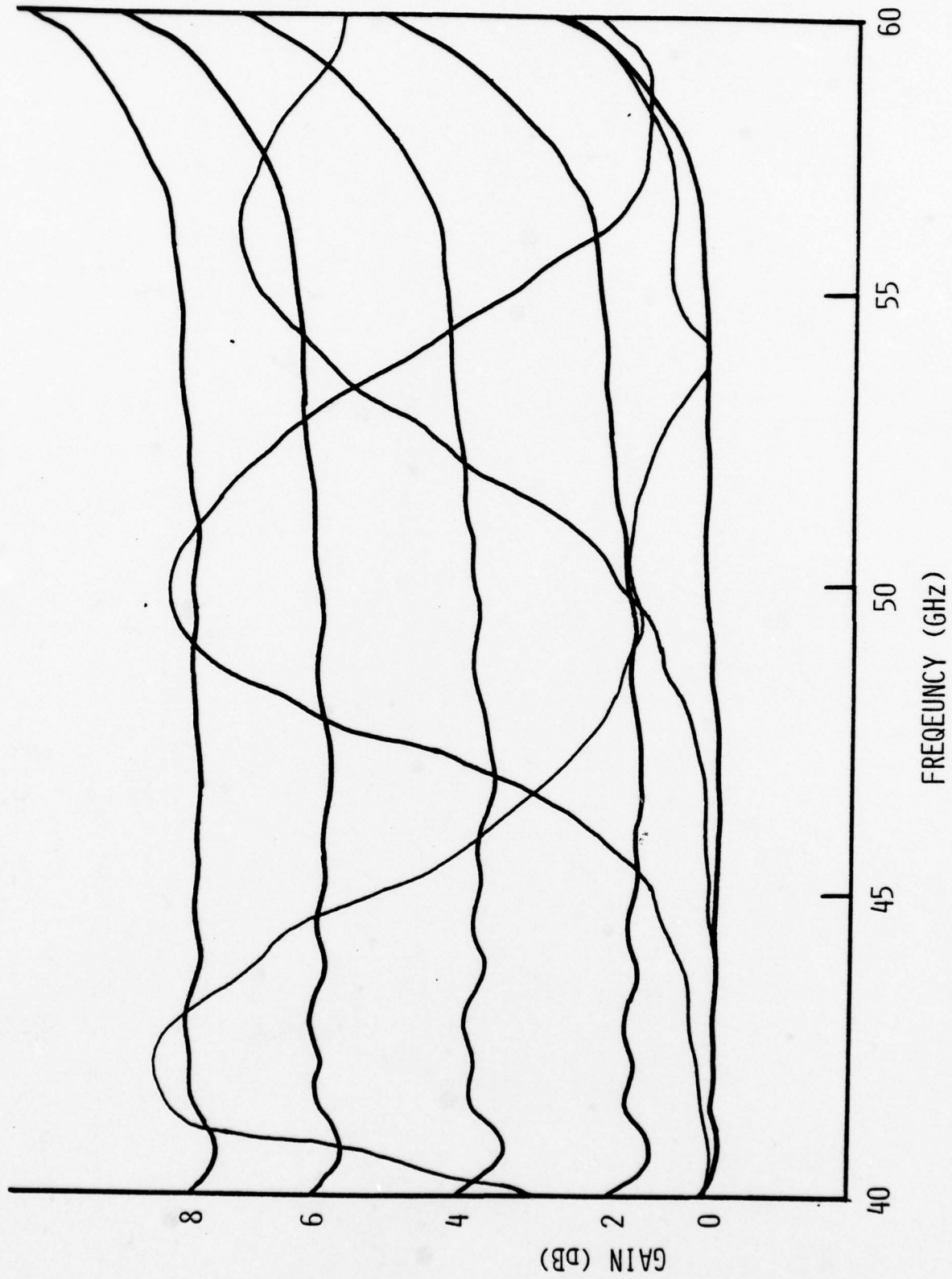


FIGURE 5.4 GAIN RESPONSES OF EE96 IN THE 43.5; 50.0 AND 56.5 GHz COAXIAL WAVEGUIDE CIRCUITS

## 5.2 Gain and Noise Figure Measurements

The Ka-band circuit used to perform gain and noise figure measurements is shown in Figure 5.5. The manual waveguide switch is shown in the position for making noise figure measurements. The noise source which is used is an ALL noise tube having an ENR of 16.3 dB, and the mixer is a Spacekom mixer FKa-U. The noise power is measured at an I.F. of 60 MHz. Noise figure measurements have been made using both the manual and automatic Y-factor methods. Agreement between both methods was good. Determination of the noise figure of the InP amplifier under test over a wide frequency range by the automatic method requires accurate measurement versus frequency of the loss of the circuit between the noise tube and the amplifier under test, the gain of the amplifier, the loss of the circuit between the amplifier and the mixer, and the noise figure of the mixer. The manual Y-factor method requires accurate measurement versus frequency of the loss of the circuit between the noise tube and the amplifier under test, as well as accurate calibration of the microwave attenuator being used. Because the gain of the InP amplifier under test at certain frequencies of interest is as low as 3 dB, the correction factors due to circuit losses and mixer noise figure are significant and must be computed. The manual Y factor method requires less correction factors, and as a result is simpler and possibly more accurate for making measurements over a wide range of frequencies and amplifier gain levels. The values of noise figure reported here for Ka-band were obtained using the manual Y factor method, and have been corrected for circuit and circulator losses.

The circuit used to perform gain and noise figure measurements in U-band is shown in Figure 5.6. A Micro-Now sweeper is used in obtaining gain measurements, but the BWO has been found to be too noisy to use as an L.O. for the Spacekom mixer in making noise figure measurements. Instead a mechanically tuned Gunn oscillator is used as an L.O. A C.P. Clare noise tube having an

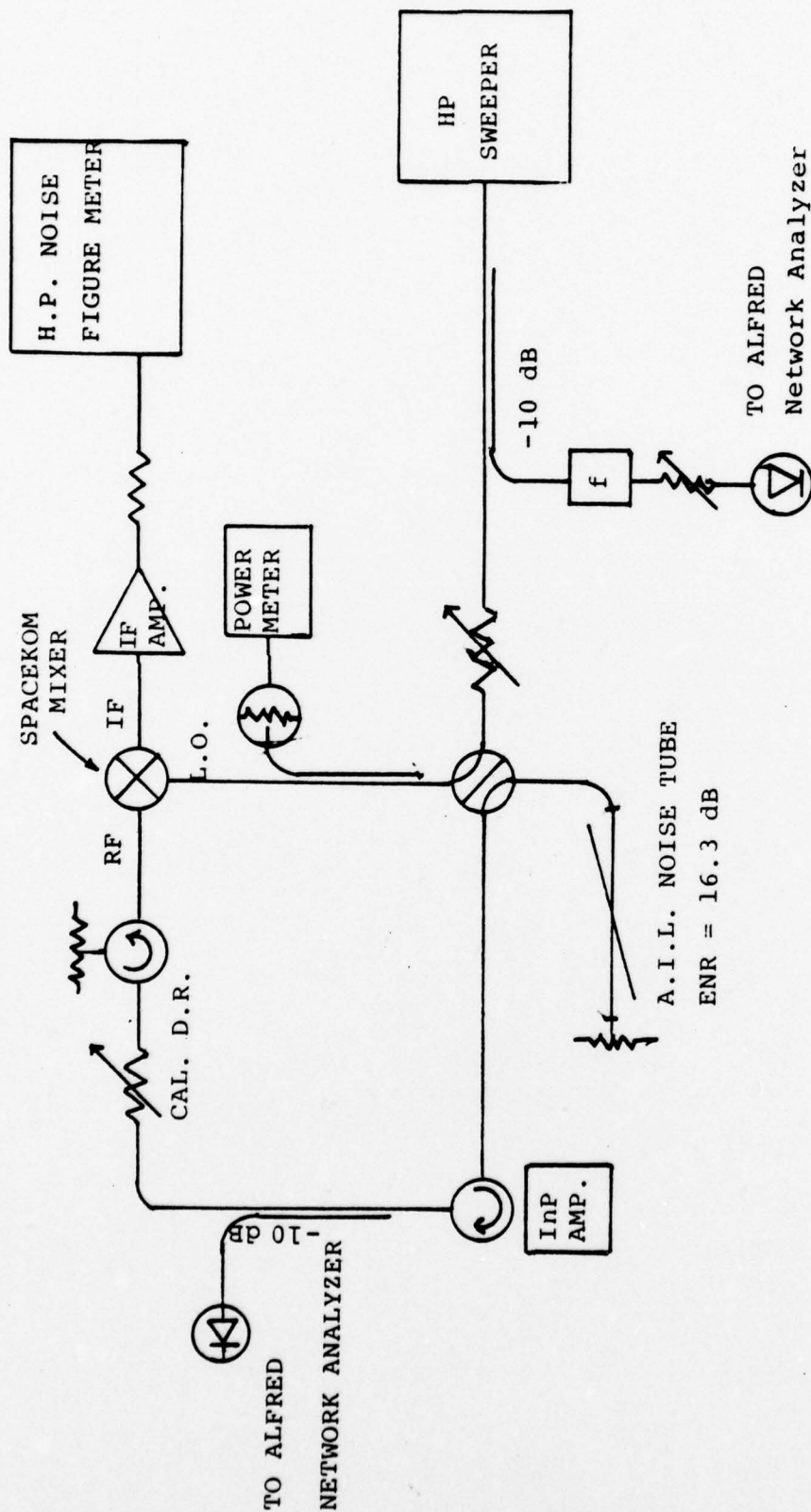


FIGURE 5.5 KA-BAND GAIN AND NOISE FIGURE MEASUREMENT CIRCUIT

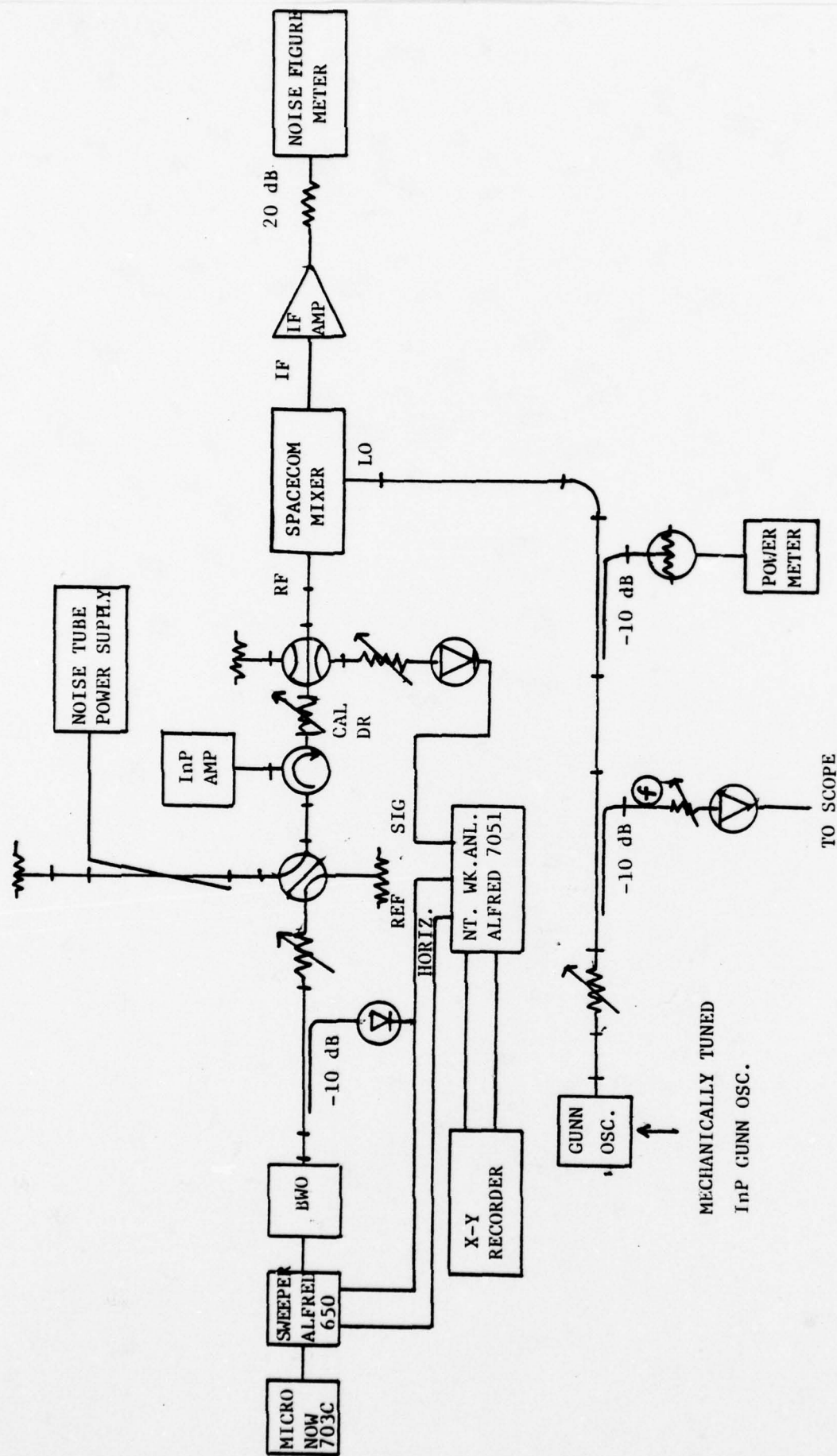


FIGURE 5.6 40-60 GHz GAIN AND NOISE FIGURE MEASUREMENT CIRCUIT

ENR of 15.4 dB is used as a noise source and the noise power is measured at an I.F. of 60 MHz. Noise figure measurements are made using the manual Y-factor method. Note that the noise figures reported here for U-band have not been corrected for circuit and circulator losses as they have been in Ka-band.

During this second reporting period, emphasis has been placed on the evaluation of the cathode notch structure for low noise amplification. There are four doping profile parameters which have significant effects on the rf performance of a notch device. The active layer length determines the transit frequency. The active layer doping-length product affects the gain and noise figure. The notch doping determines the gradient of the electric field through the notch region; the length of the notch determines the electric field level at the active-layer-notch interface. Thus, the notch parameters determine the uniformity of the electric field in the active region, affecting the noise figure of the device. The length of the notch also has an effect on the gain of the device. It adds a resistance in series with the negative resistance of the active layer, effectively, reducing the gain of the device if its length becomes too great.

A series of notch wafers have been grown in which these four parameters have been varied in order to determine the optimum values for low noise operation throughout the 26.5-60 GHz range. Thirteen cathode notch wafers were evaluated in this reporting period. Table 5.1 lists the four main doping profile parameters of each wafer as well as the rf performance data for each wafer. The active layer doping level varied over the length of the active layer for several of these wafers. The magnitude of the gradient can be determined from the range of doping given in Table 5.1. The rf data reported in Table 5.1 represents the performance of a typical device from a given wafer in one of the test circuits. The maximum and minimum gain and noise figures are given for a specified frequency interval bounded by the indicated range.

WAFER	SSW RUN NO	ACTIVE		NOTCH		FREQUENCY		GAIN		NOISE FIGURE	
		n (cm <sup>-3</sup> )	L (um)	n (cm <sup>-3</sup> )	L (um)	Interval (GHz)	Range (GHz)	Max (dB)	Min (dB)	Max (dB)	Min (dB)
EE115	51-2	1.2-1.8x10 <sup>15</sup>	6.2	3.2x10 <sup>14</sup>	1.8	2.5	26.5-28	6.0	3.0	13.1	11.9
EE116	51-3	1.1-2.0x10 <sup>15</sup>	5.0	2.4x10 <sup>14</sup>	1.6	7.0	26.5-33.5	7.0	4.0	12.5	9.6
EE117	52-9	0.9x10 <sup>15</sup>	3.2	4.8x10 <sup>13</sup>	2.4	2.3	29.2-31.5	5.0	3.0	8.3	7.4
EE118	53-2	2.1-3.7x10 <sup>15</sup>	3.9	2.0x10 <sup>14</sup>	1.7	4.5	31.0-35.5	10.0	6.0	14.3	11.5
EE119	53-4	1.2-1.8x10 <sup>15</sup>	4.6	5.1x10 <sup>13</sup>	1.7	6.6	29.6-36.2	10.0	6.0	11.8	11.1
EE120	53-5	5.6-6.2x10 <sup>14</sup>	3.9	3.2x10 <sup>13</sup>	2.5	4.2	29.8-34.0	6.5	4.0	8.3	7.1
EE121	53-6	1.0-1.05x10 <sup>15</sup>	2.1	3.1x10 <sup>13</sup>	2.8	4.8	33.4-38.2	6.0	3.0	8.5	6.8
EE122	53-7	7.0-8.4x10 <sup>14</sup>	2.3	6.2x10 <sup>13</sup>	1.7	3.5	34.0-37.5	4.0	4.0	7.9	7.1
EE123	54-3	.94-1.1x10 <sup>15</sup>	0.7	2.0x10 <sup>14</sup>	1.0	4.6	42.6-47.2	5.0	2.0	10.1	7.7
EE124	54-5	1.2-1.3x10 <sup>15</sup>	1.8	5.6x10 <sup>13</sup>	1.8	2.4	34.2-36.6	4.0	3.0	8.3	6.7
EE125	54-7	1.7-2.2x10 <sup>15</sup>	1.7	7.7x10 <sup>13</sup>	1.5	---	40-60	no gain		---	---
EE126	54-8	1.0-1.2x10 <sup>15</sup>	1.7	1.05x10 <sup>14</sup>	1.6	1.5	43-44.5	9.5	6.0	10.1	8.6
EE127	54-9	3.5-4.6x10 <sup>14</sup>	2.4	5.7x10 <sup>13</sup>	1.8	4.7	33.6-38.3	5.0	3.0	9.6	8.3
						2.5	43-45.5	11.0	6.0	11.2	9.6
						4.5	33-37.5	5.0	3.0	8.8	7.0
						2.5	42.5-45	8.0	4.0	9.8	7.9
						4.0	34-38	4.0	3.0	7.1	6.3
						4.0	34-38	3.0	2.0	6.3	5.4
						2.5	42.3-44.8	6.0	3.0	8.8	6.9

TABLE 5.1

DOPING PROFILE PARAMETERS AND RF PERFORMANCE OF NEW CATHODE NOTCH WAFERS

The best low noise performance in Ka-band was achieved with wafers EE120, EE121, and EE127. Figure 5.7 shows the gain response and noise figures of EE120 in the lower end of Ka-band; maximum noise figure was 8.3 dB with a gain greater than 6.0 dB. In the upper end of Ka-band, EE121 performed very well as shown in Figure 5.8; maximum noise figure was less than 8.0 dB with gains as high as 5.5 dB. Low noise performance was achieved with EE127 in upper Ka-band. Results for typical devices from this wafer are shown in Figure 5.9; maximum noise figure is 7.1 dB and peak gain is 4.0 dB. A few devices from this wafer gave very low noise figures with somewhat lower gain. As shown in Figure 5.10 noise figures ranging from 5.4 dB to 6.3 dB were measured for gain of approximately 3 dB. Higher gain with a corresponding increase in noise figure can be achieved by using devices with greater active layer doping levels. As an example, the gain response of EE119 is shown in Figure 5.11. Gain of 10 dB with noise figures less than 12.0 dB was measured. Higher doped wafers such as EE119 will be useful in second or third stage amplifiers.

The best low noise performance in U-band was obtained from EE127. Typical gain response and noise figures in the 43.5 GHz circuit are shown in Figure 5.12, maximum noise figures which were less than 9.0 dB were obtained with a peak gain of nearly 6 dB. Again, higher gain can be achieved by using higher doped devices but noise figure is sacrificed. As an example, Figure 5.13 shows the gain response of EE126, which had an active doping three times greater than EE127. Maximum noise figures were less than 10 dB with 8 dB peak gain.

### 5.3 Circuit Development

In order to construct a staggered gain, full band amplifier for Ka-band, it will be necessary to have 6 dB of gain over a 7 GHz bandwidth. The best low noise results to date have been accompanied with low gain (6 dB or less) and bandwidths on the order of 4 GHz. These results have been achieved with cathode notch devices which have low active layer dopings.

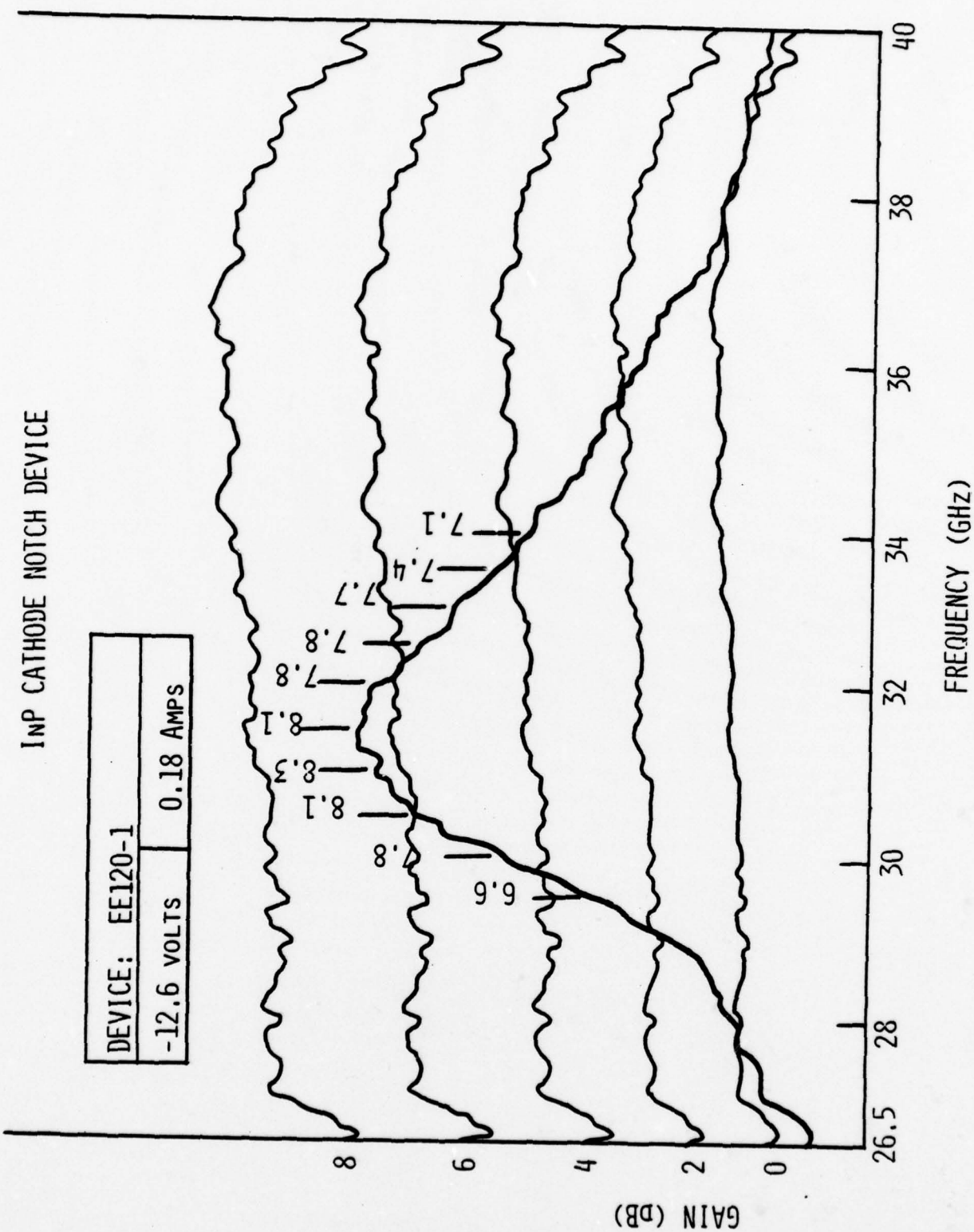
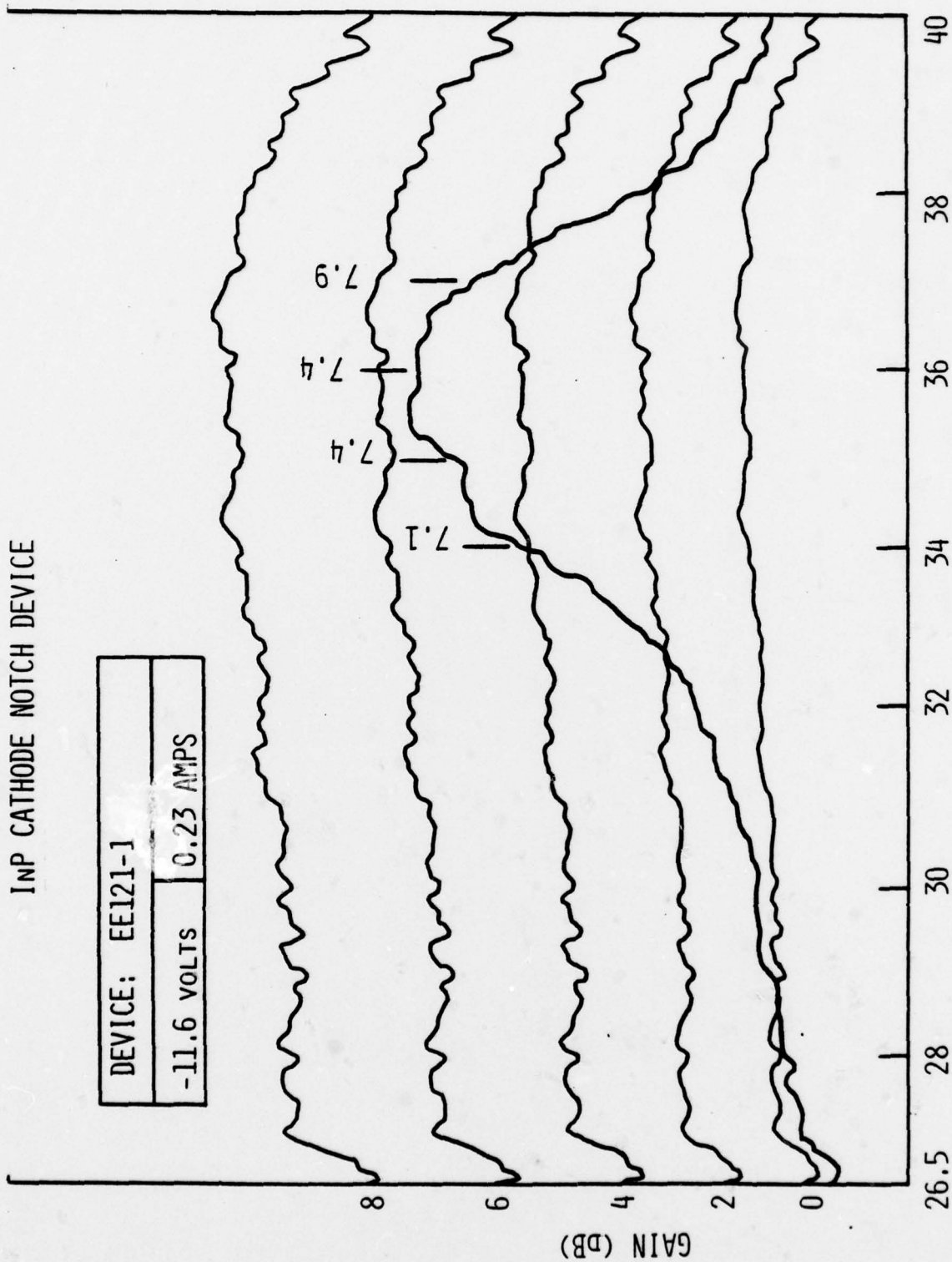


FIGURE 5.7 TYPICAL GAIN AND NOISE FIGURES OF EE120

# INP CATHODE NOTCH DEVICE

DEVICE: EE121-1	
-11.6 VOLTS	0.23 AMPS



FREQUENCY (GHz)

FIGURE 5.8 TYPICAL GAIN AND NOISE FIGURES OF EE121

# INP CATHODE NOTCH DEVICE

DEVICE: EE127-4	
-13.5 VOLTS	0.29 AMPS

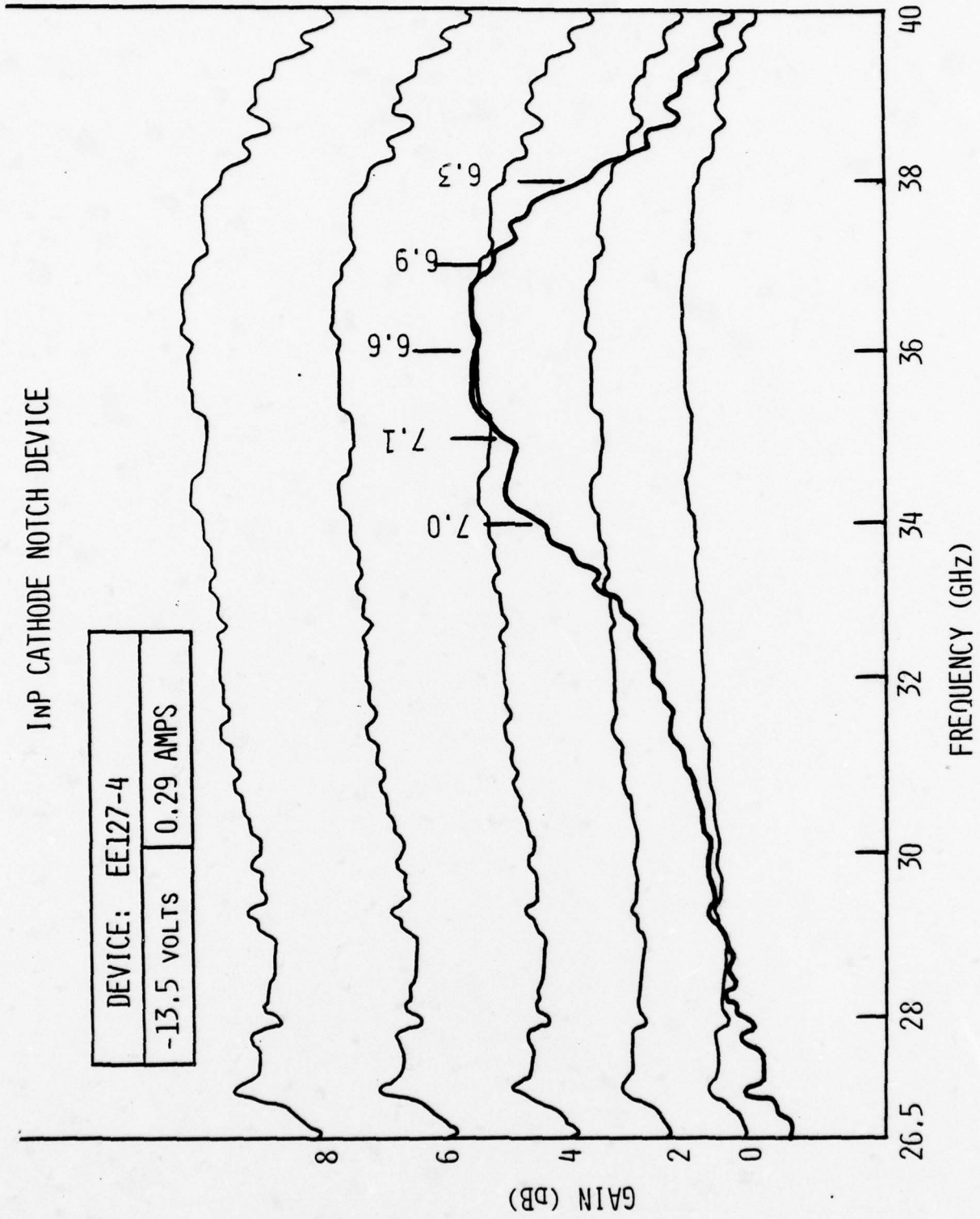


FIGURE 5.9 TYPICAL GAIN AND NOISE FIGURES OF EE127

# INP CATHODE NOTCH DEVICE

DEVICE: EE127-1	
-14.1 VOLTS	0.26 AMPS

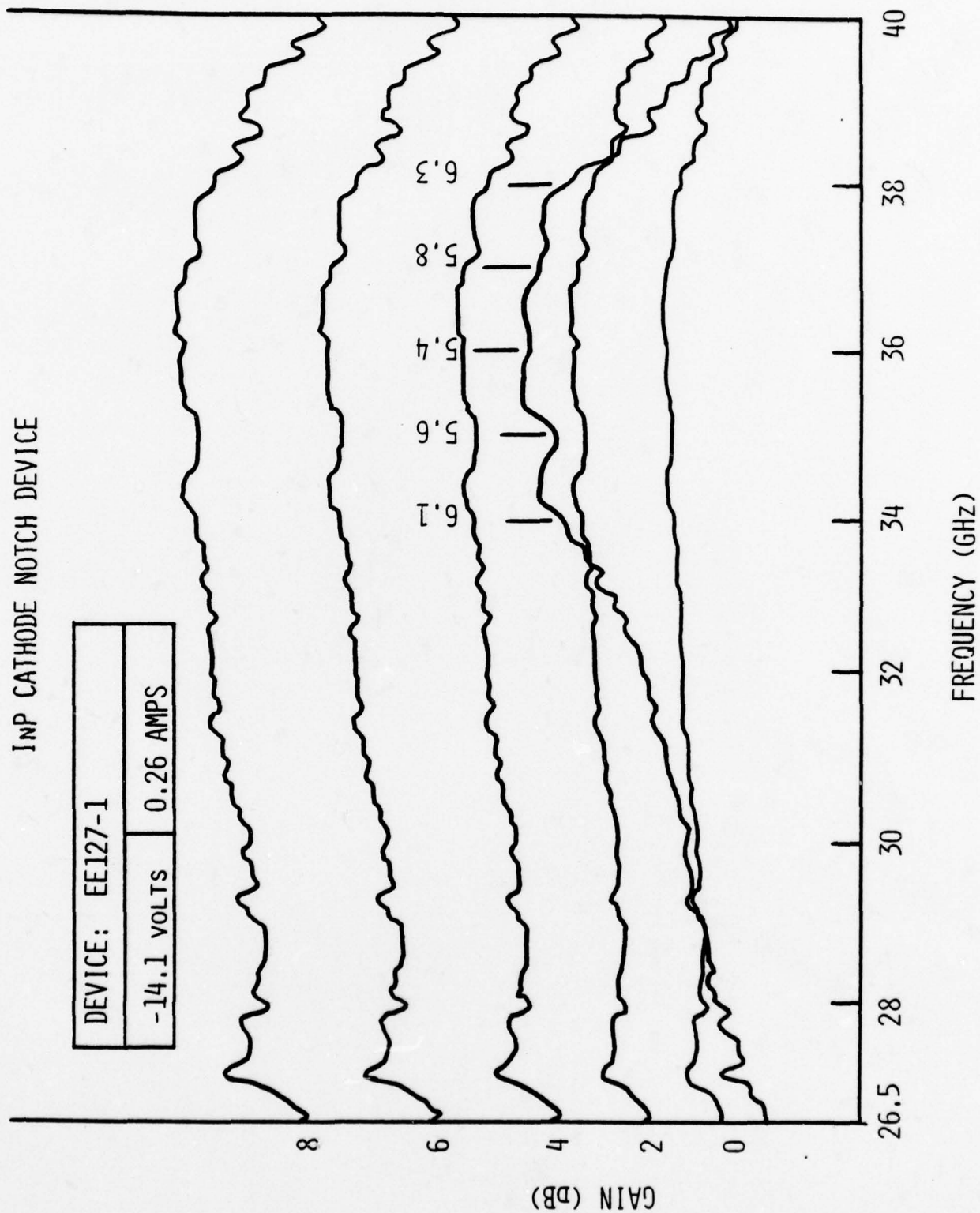


FIGURE 5.10 BEST LOW NOISE PERFORMANCE OF EE127

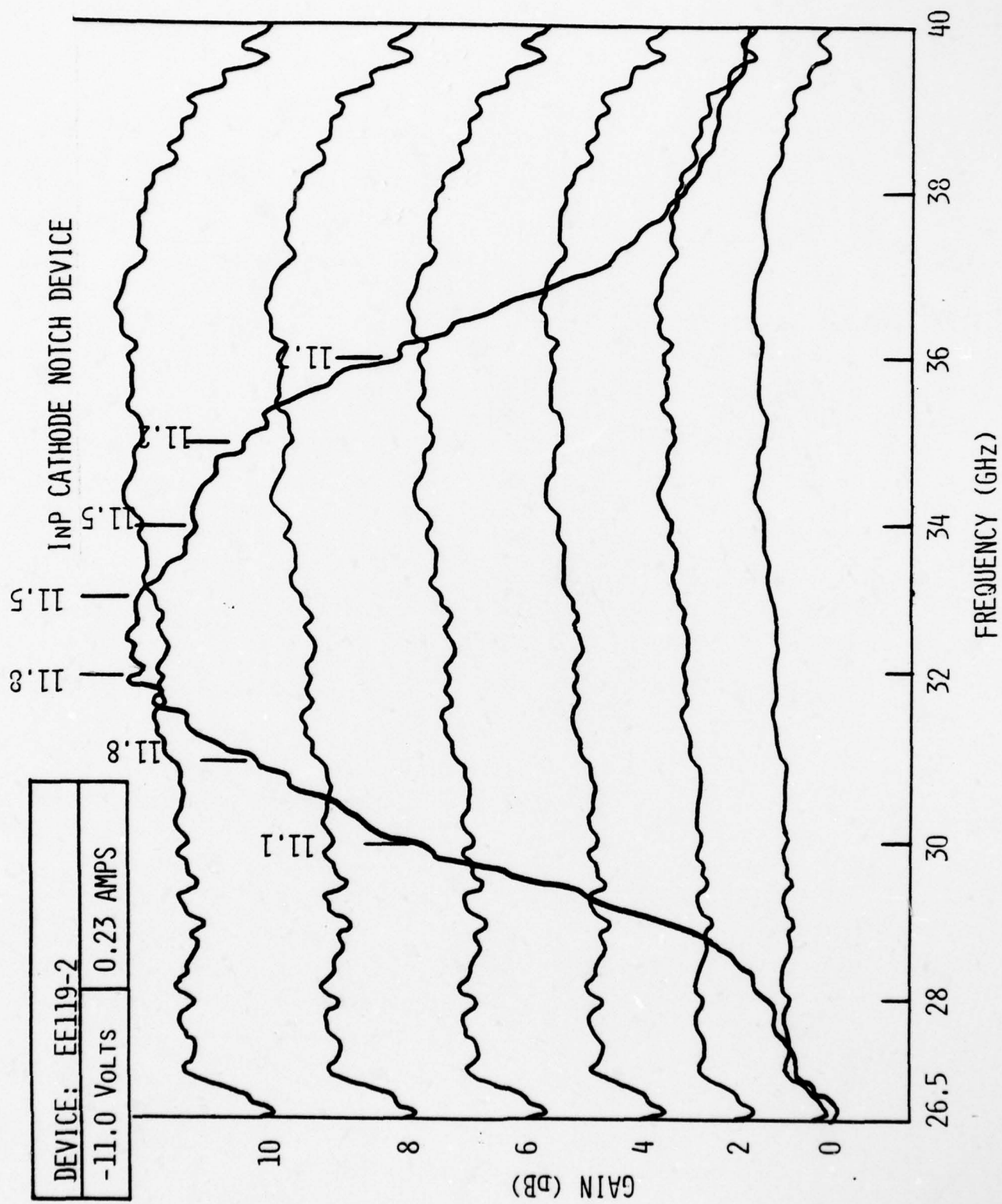


FIGURE 5.11 TYPICAL GAIN AND NOISE FIGURES OF EE119

# INP CATHODE NOTCH DEVICE

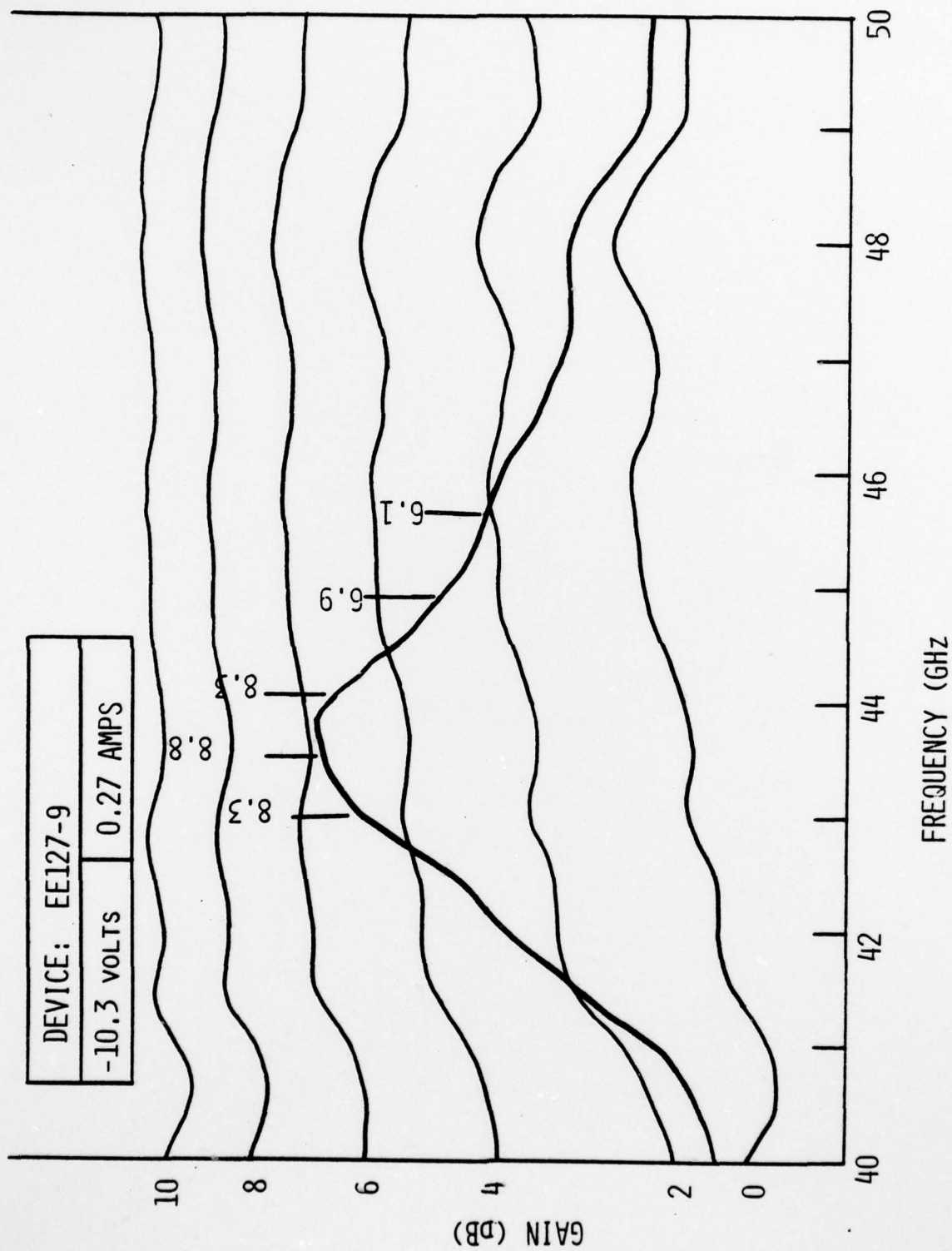
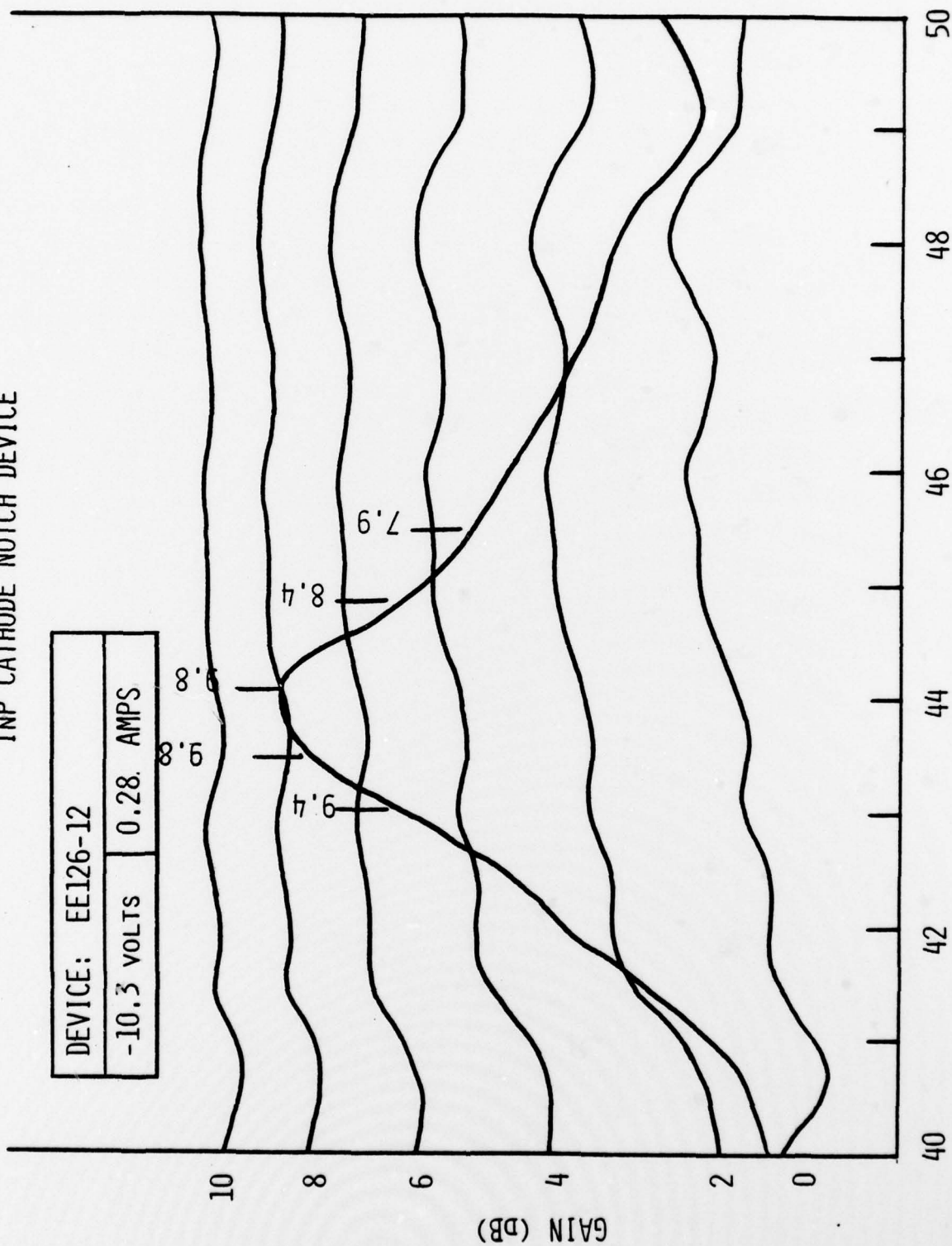


FIGURE 5.12 TYPICAL GAIN AND NOISE FIGURES OF EE127

# INP CATHODE NOTCH DEVICE



FREQUENCY (GHz)

FIGURE 5.13 TYPICAL GAIN AND NOISE FIGURES OF EE126

Modifications of the coax-waveguide circuit will be necessary in order to achieve greater gain and bandwidth. The main parameters which affect the performance of this circuit are: a) characteristic impedance of coaxial section,  $Z_0$ ; b) length of coaxial section,  $L$ ; c) recess of diode flange into heat sink; and, d) dimensions of waveguide-to-coax transforming section.

A variety of coaxial sections having different characteristic impedances and length combinations were constructed for the 37.0 GHz circuit. The various combinations are shown in Figure 5.14 where the length,  $L$ , has been normalized to the free space wavelength,  $\lambda_0$ , at 37.0 GHz. The characteristic impedance was varied by changing the diameter,  $D$ , of the center conductor. Curves A, B, C, and D of Figure 5.15 are the gain responses of EE120 for 52, 40, 30 and 20 ohm coaxial sections, respectively, with  $L/\lambda_0$  held constant. EE120 is a cathode notch wafer with low active doping. Lowering of the coaxial impedance increased the gain but lowered the center frequency and significantly decreased the bandwidth. Note the bias of the diode was lowered in the case of the 30 and 20 ohm chokes in order to limit the gain to less than 12 dB.

As shown in Figure 5.16 the InP packaged diode terminating the end of the coaxial air line may be represented by the accompanying equivalent circuit.  $C_1$ ,  $C_2$  and  $L_1$  are fringing capacitances and a parasitic inductance associated with corner effects.  $C_r$  and  $L_r$  are the capacitance and inductance associated with the radial line surrounding the diode. Changes in the dimension,  $D$ , not only affect the circuit impedance presented to the diode,  $Z_a$ , but also significantly change these parasitic elements surrounding the diode, causing significant changes in the impedance at the plane of the diode which is seen by the circuit,  $Z_b$ . The changes in the gain responses of Figure 5.15 produced by varying the diameter,  $D$ , result from changes in  $Z_b$  as well as in  $Z_a$ .

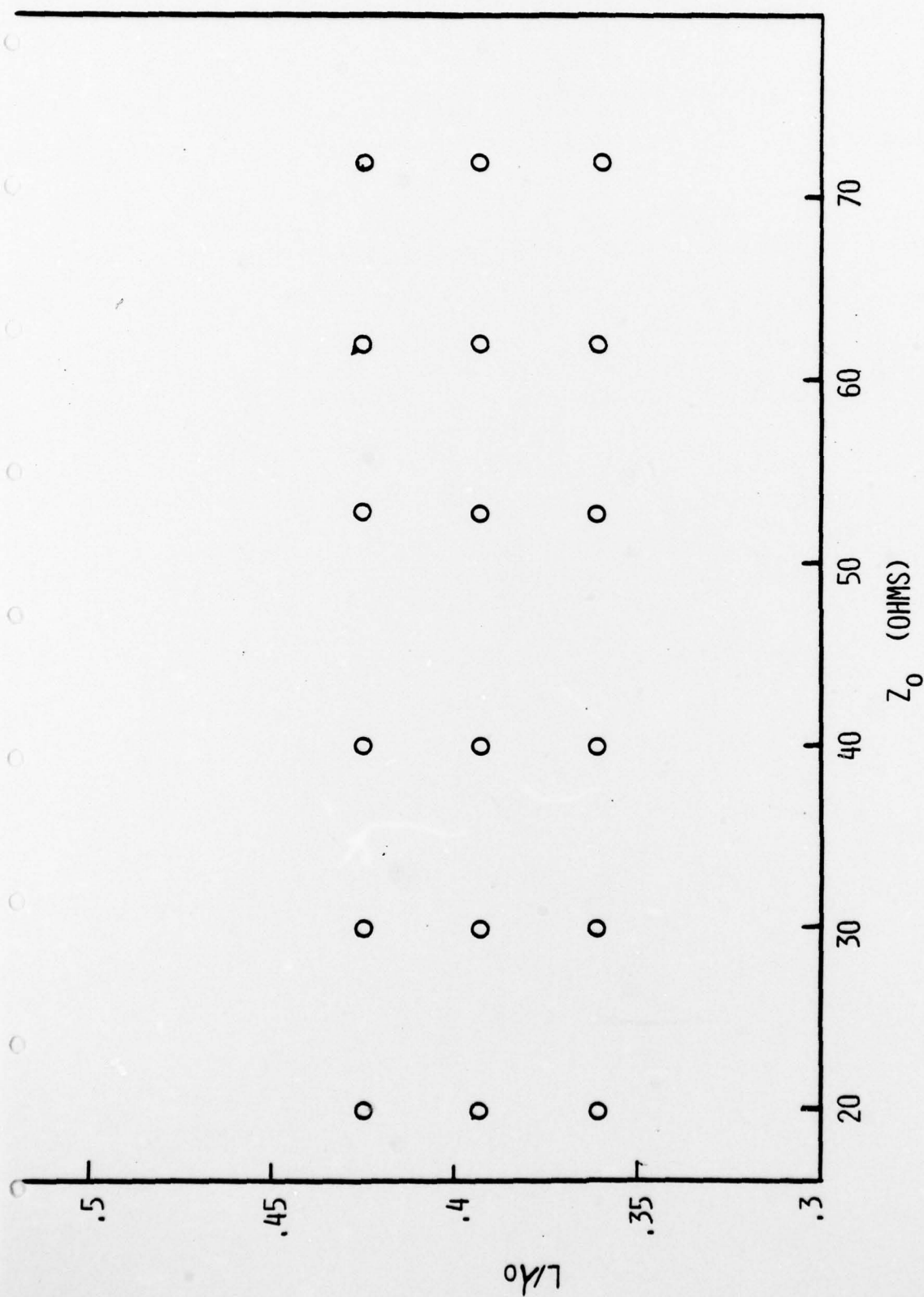


FIGURE 5.14 NORMALIZED LENGTH AND CHARACTERISTIC IMPEDANCE COMBINATIONS OF COAXIAL SECTIONS USED IN TUNING 37.0 GHz CIRCUIT

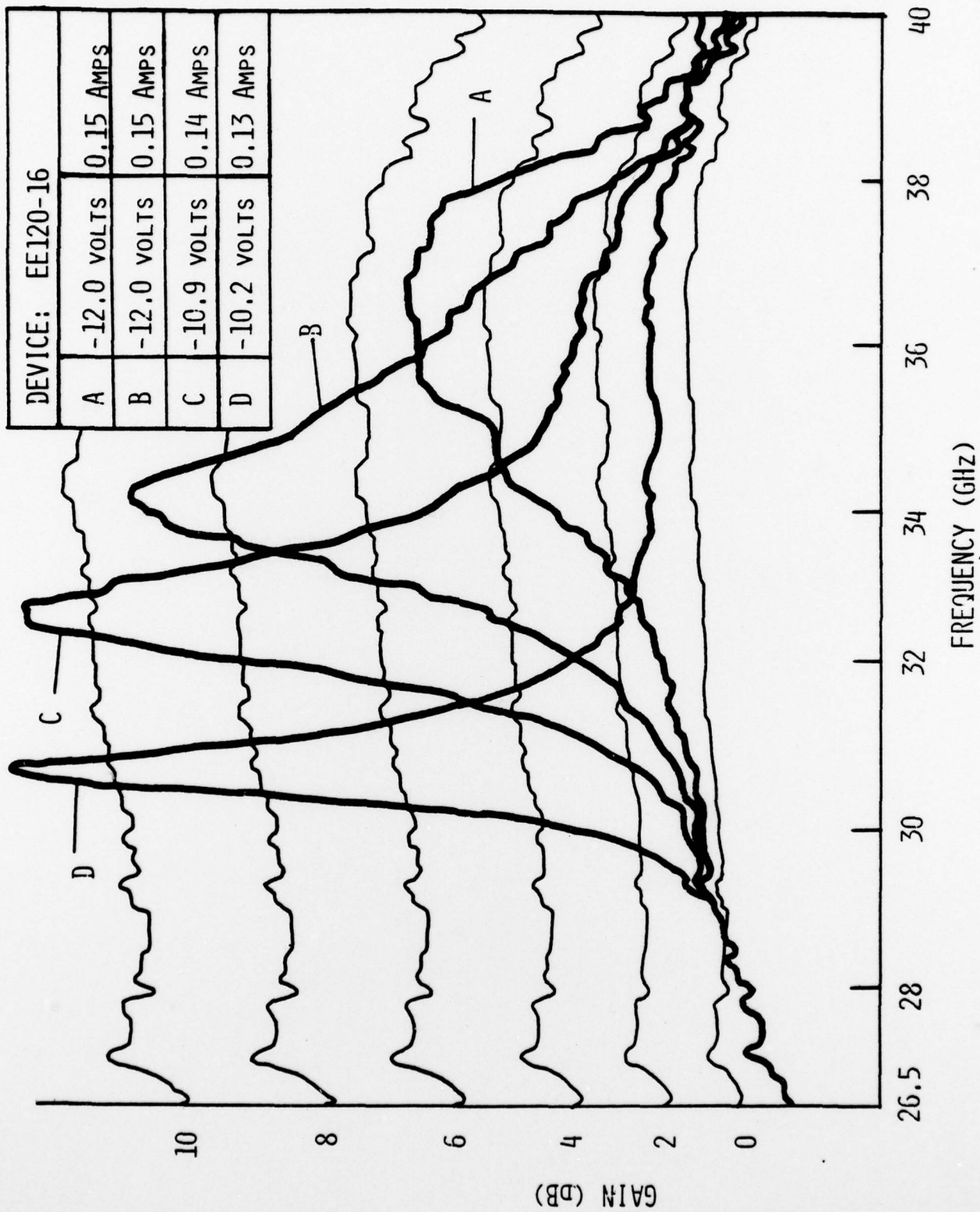
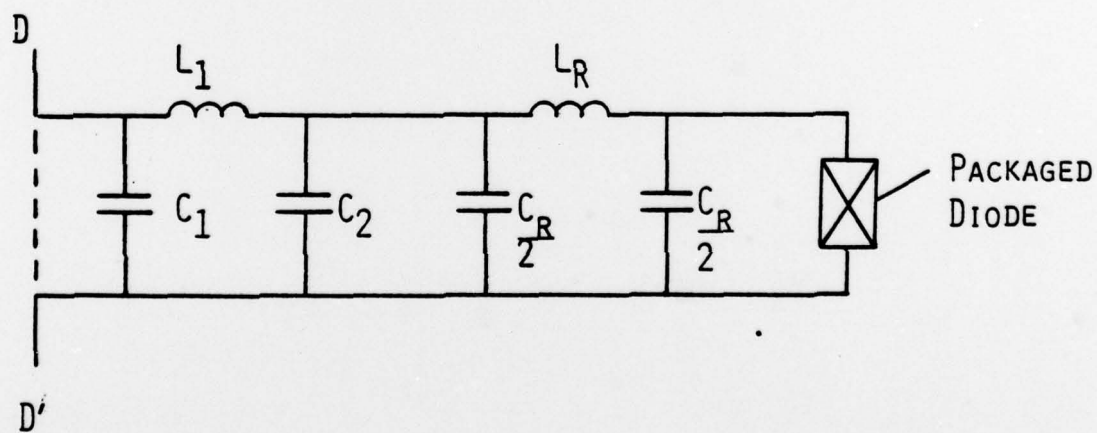


FIGURE 5.15 GAIN RESPONSES FOR COAXIAL SECTIONS OF DIFFERENT IMPEDANCES



55

The impedance of the circuit,  $Z_a$ , and the impedance at the plane of the diode,  $Z_b$ , can be determined using de-embedding techniques. The Ka-band network analyzer and a de-embedding computer program are now operational, and are being used to study the effects of varying the diameter and length of the coaxial section on the impedances  $Z_a$  and  $Z_b$ , and from this information the effects on the gain response.

In order to perform the de-embedding calculations, the measurement of at least three reflection coefficients at the input plane of the intervening circuit is required for three known load impedances at the output port of the intervening circuit. This allows the calculation of the scattering matrix of this intervening circuit or equivalently the impedance presented at this plane by the circuit. A measurement of a fourth reflection coefficient at the input plane with the diode in place will allow calculation of the impedance at the plane of the diode. For the coaxial-waveguide circuit under consideration here, the input plane of the intervening circuit is plane CC' of Figure 5.17. The three known load impedances presented to the circuit at plane DD' are offset coaxial shorts of three different lengths,  $L_1$ ,  $L_2$  and  $L_3$ . The center conductor diameter of these offset shorts is equal to the center conductor diameter of the choke being used.

Preliminary results showing  $Z_a$  versus frequency and  $-Z_b$  versus frequency are plotted on the Smith chart of Figure 5.18 for a cathode notch device in the 38.0 GHz circuit.  $Z_b$  has a real part which varies from -4.3 ohms to -8 ohms in the frequency range from 29 to 40 GHz. From these results, the gain versus frequency was calculated and is shown in Figure 5.19 along with the swept gain measured for this same diode under the same bias conditions. Agreement is reasonably good indicating the computer program and measurements are working properly.

Detailed measurements of  $Z_a$  and  $Z_b$  for different center conductor diameters and lengths will be performed in the 37.0 GHz circuit. Offset shorts have been constructed for the 37.0 GHz circuit which will allow measurements of  $Z_a$  and  $Z_b$  for coaxial sections having characteristic impedances of 20, 40 and 62 ohms.

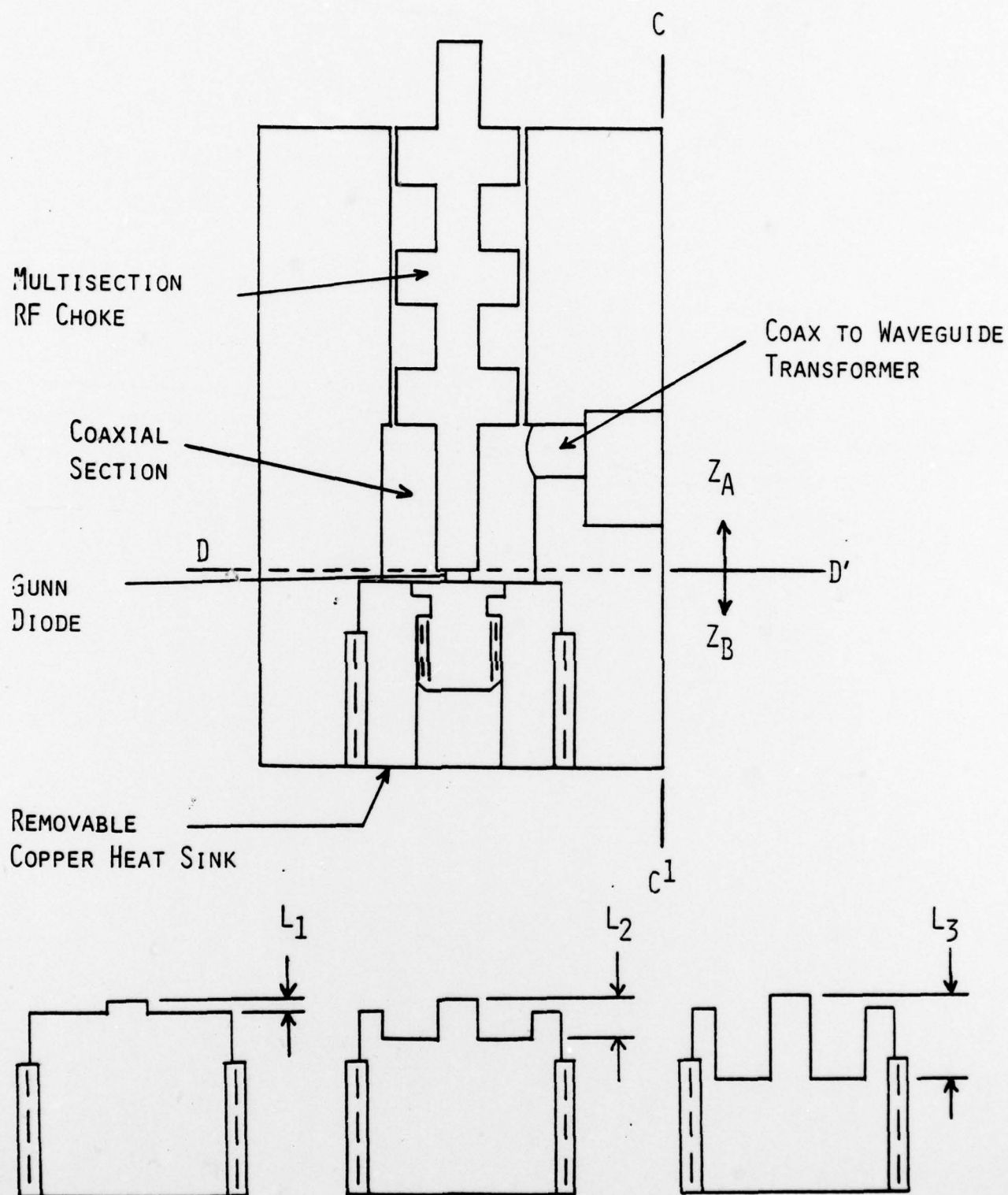


FIGURE 5.17 COAXIAL-WAVEGUIDE CIRCUIT AND THREE KNOWN LOAD IMPEDANCES USED FOR DE-EMBEDDING

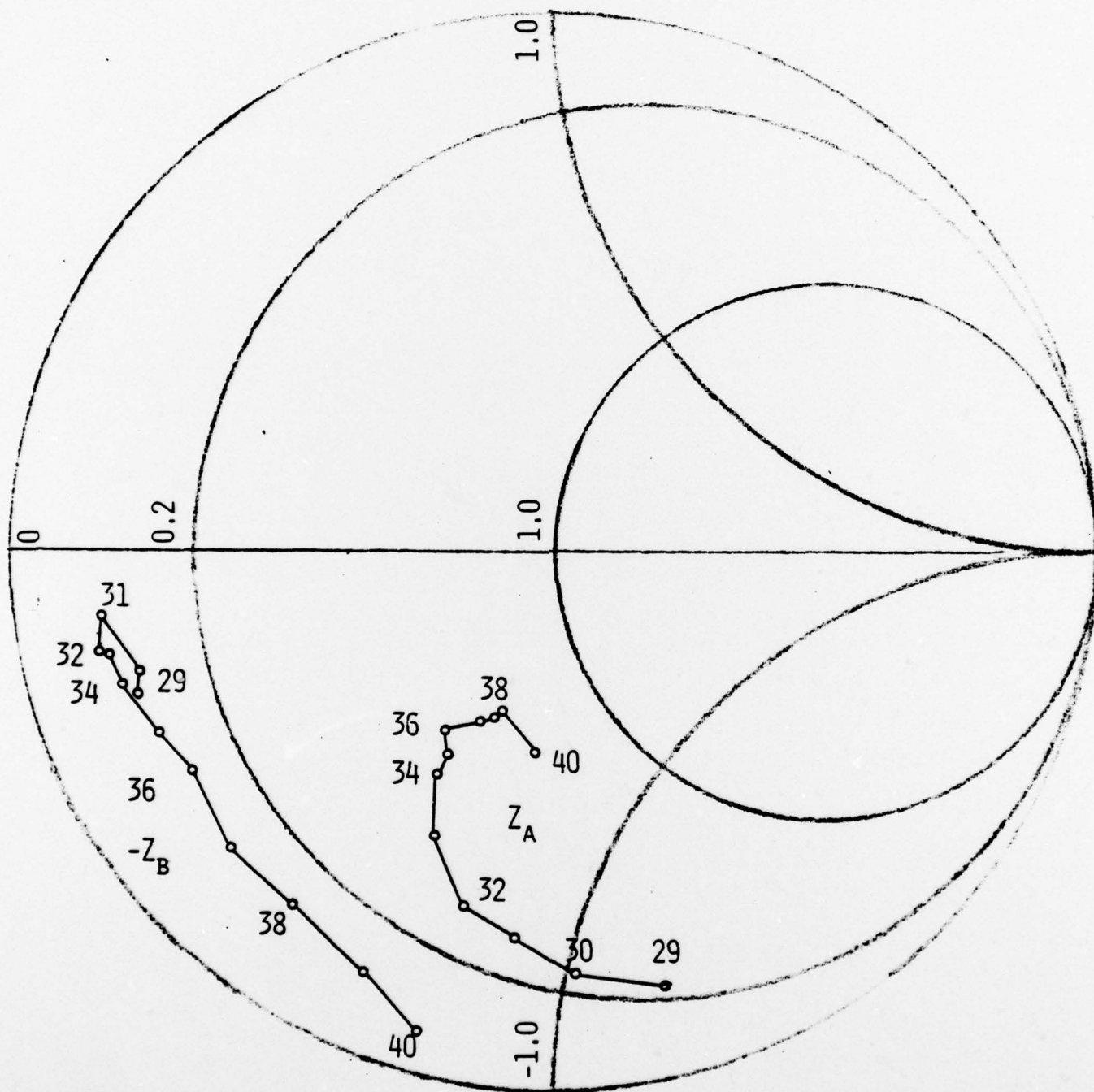


FIGURE 5.18 MEASURED 38.0 GHz CIRCUIT IMPEDANCE AND NEGATIVE OF EE120 DIODE IMPEDANCE

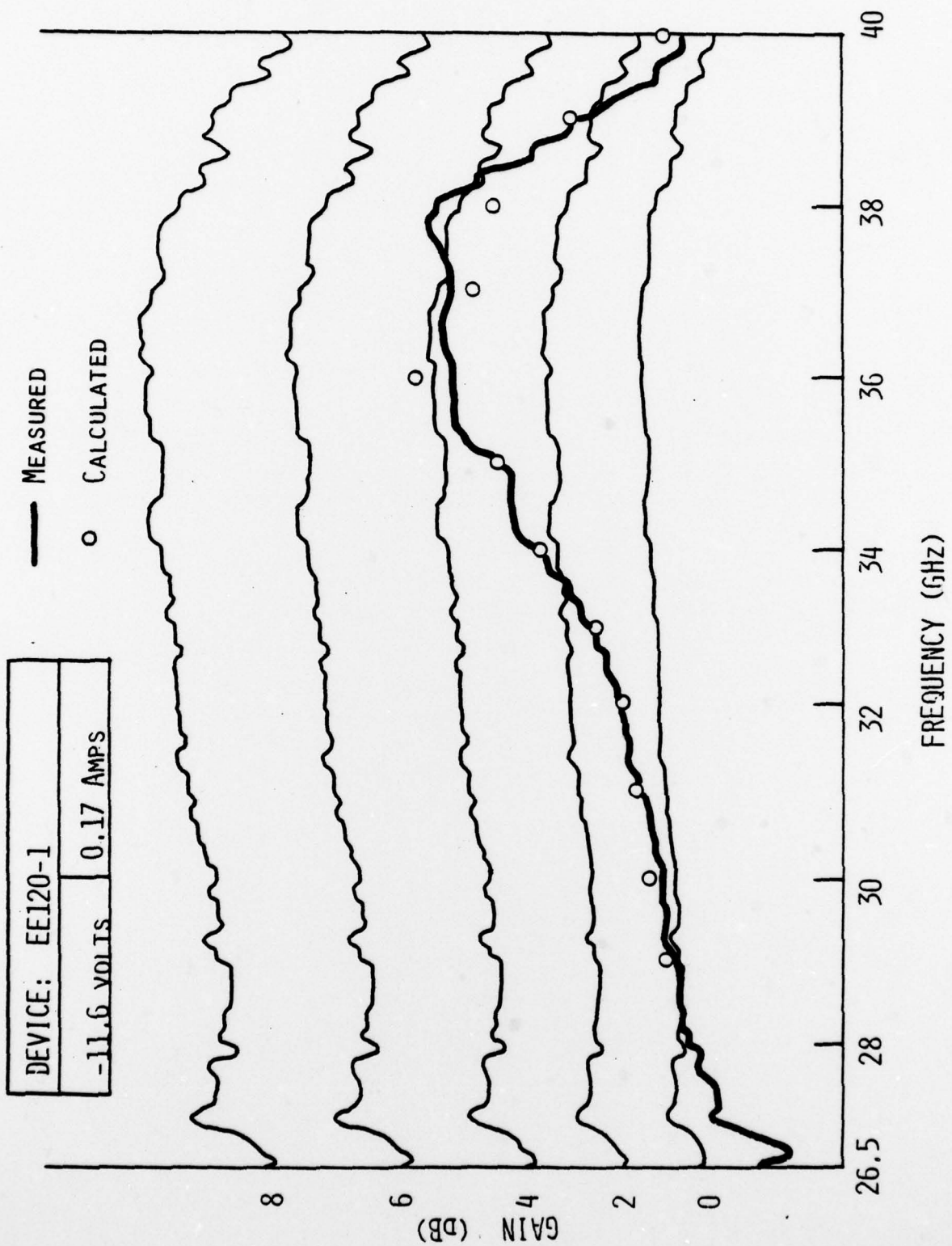


FIGURE 5.19 MEASURED AND CALCULATED GAIN OF NOTCH DEVICE

Extensive measurements performed in U-band (40-60 GHz) have indicated several trends. Figure 5.20 shows the gain responses of a device from a cathode notch wafer EE125 and a device from a three layer wafer EE96. Both wafers had approximately equal active layer doping,  $n = 1.7-2.2 \times 10^{15} \text{ cm}^{-3}$  for EE 125 and  $n = 1.8-2.0 \times 10^{15} \text{ cm}^{-3}$  for EE96. Active layer thickness of EE125 was 1.7  $\mu\text{m}$  and of EE96 was 3.2  $\mu\text{m}$ . This data indicates that cathode notch devices having active layer dopings which are comparable to a three layer device can give as wide a bandwidth response. The notch device should have a more uniform field in the active region, and therefore does not require as long an active layer to operate at a given frequency. Noise figure measurements on EE96 and EE125 at 45 GHz show the notch device having noise figures which are lower by at least 3 dB for comparable gain levels.

Figure 5.21 demonstrates the circuit impedance required to obtain high gain from a highly doped three layer device EE96 is by no means optimum for a lower doped notch device such as EE124. Curve A is for EE96 in the 50 GHz circuit; curve B is for EE124 in the same circuit with bias adjusted for maximum gain. Gain of only 3 dB was obtained from EE124 whereas 8 dB was obtained from EE96. However, if the center conductor length is increased, the gain from EE124 can be increased to 5 dB, accompanied by a shift to a lower center frequency, as in curve C.

In general, notch wafers with low active layer dopings tend to operate at lower frequencies than a heavily doped notch or three layer device when the center conductors are selected for maximum gain. Gain increases with device area for these low doped notch devices, but the center frequency also shifts to a lower frequency as device area increases. Measurements of circuit and diode impedance on a variety of diodes in Ka-band should give some insight into the effects of lowering the active layer doping level of a notch device and also allow the determination of the optimum circuit impedance.

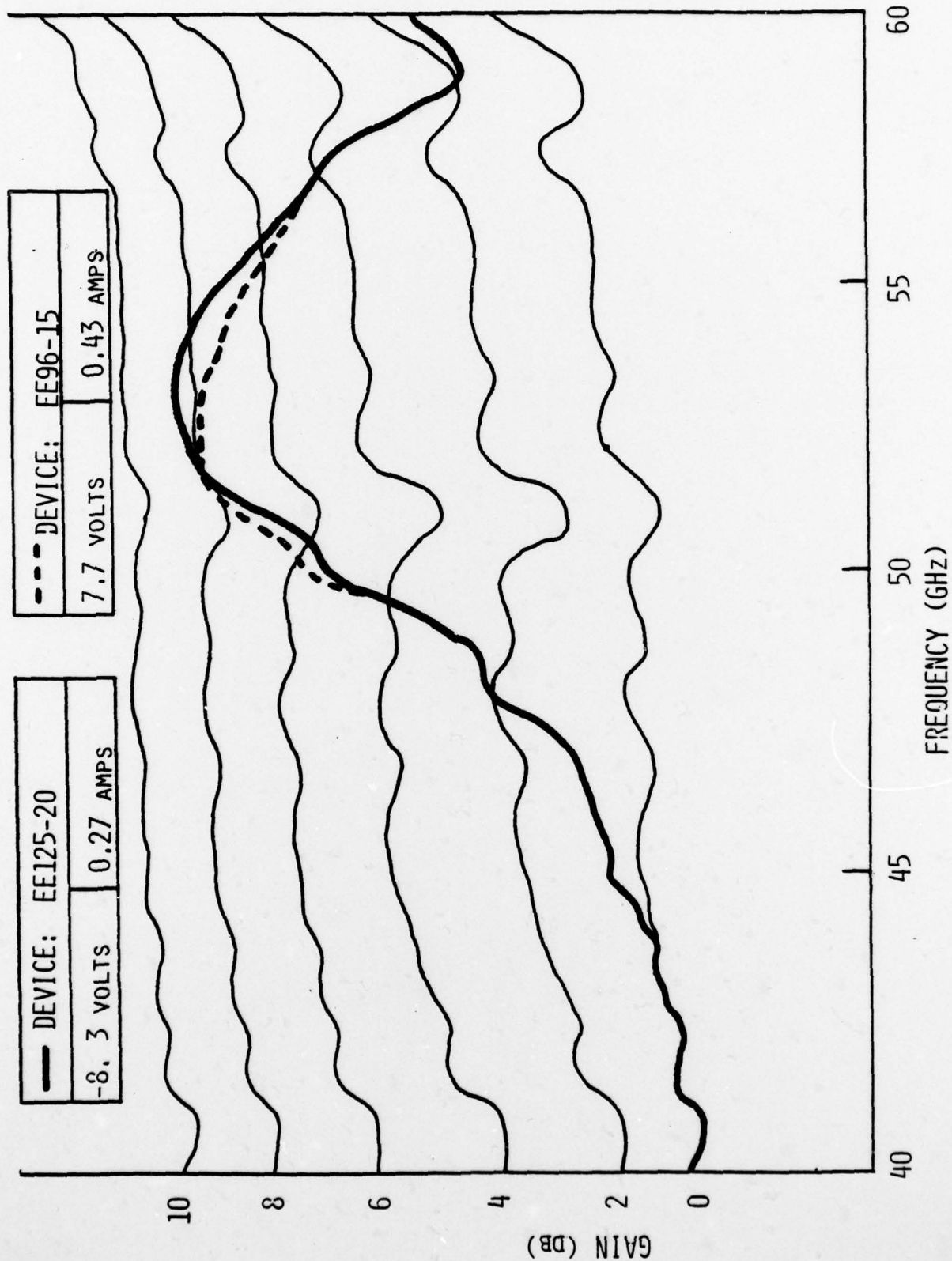


FIGURE 5.20 GAIN RESPONSES OF NOTCH WAFER, EE125, AND THREE LAYER WAFER, EE96

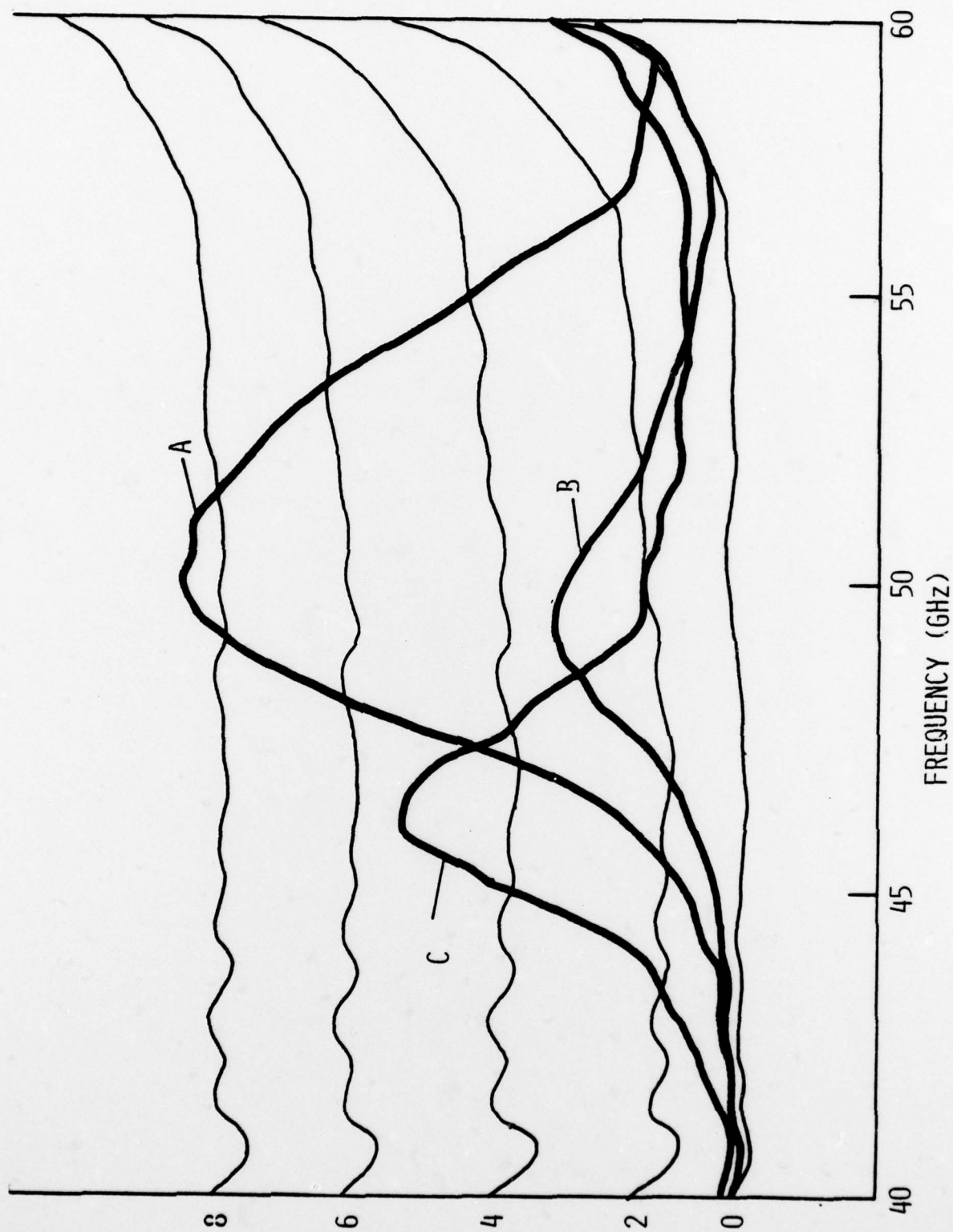


FIGURE 5.21 COMPARISON OF GAIN RESPONSES OF LOW DOPED NOTCH DEVICE AND HIGH DOPED THREE LAYER DEVICE

## 6. FUTURE PLANS

- 6.1 VPE growth of optimum cathode notch wafers for the low end of Ka-band.
- 6.2 VPE growth of cathode notch wafers in which the notch width is varied with other parameters held constant.
- 6.3 Completion of measurements of diode and circuit impedances using Ka-band network analyzer.
- 6.4 Construction of final amplifiers.

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